PREPARED BY :	SHARP	SPEC No. LCY-1315802C
		FILE No.
CHECKED BY :	DISPLAY DEVICE BUSINESS DIVISION SHARP CORPORATION	ISSUE : 11. May. 2016
		PAGE : 36 pages
	Technical Document	APPLICABLE GROUP DISPLAY DEVICE BUSINESS DIVISION

Device Datasheet and technical information for

TFT-LCD module

MODEL No. **LS029B3SX01**

RECORDS OF REVISION

MODEL NO：LS029B3SX01

SPEC NO: LCY-1315802

DATE	REVISED	PAGE	SUMMARY	NOTE
2015.08.26		—	First Issue	—
2015.08.31	A	21	Table 14	
2015.09.29	B	7	Update Table.2	
		8	Add “outside circuit”	
		28	Add “FPC schematic”	
		etc	Others	
2016.05.11	C	30	Update “Outline dimensions”	
		etc	Others	

NOTICE

○ These specification sheets are the proprietary product of SHARP CORPORATION (SHARP) and include materials protected under copyright of SHARP. Do not reproduce or cause any third party to reproduce them in any form or by any means, electronic or mechanical, for any purpose, in whole or in part, without the express written permission of SHARP.

○ The application examples in these specification sheets are provided to explain the representative applications of the device and are not intended to guarantee any industrial property right or other rights or license you to use them. SHARP assumes no responsibility for any problems related to any industrial property right of a third party resulting from the use of the device.

○ The device listed in these specification sheets was designed and manufactured for use in Telecommunication equipment (terminals)

○ In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

○ Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

○ SHARP assumes no responsibility for any damage resulting from the use of the device which does not comply with theinstructions and the precautions specified in these specification sheets.

○ Contact and consult with a SHARP sales representative for any questions about this device.

[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators
Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.
② Equipment and containers
Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.
③ Floor
Floor is an important part to leak static electricity which is generated from human body or equipment.
There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the counter measure (electrostatic earth:$1\times10^{8}\Omega$) should be made.
④Humidity
Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.
⑤Transportation/storage
Storage materials must be anti-static to prevent causing electrostatic discharge.
⑥Others
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.

(15) Do not touch the COG‘s patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

[For operating LCD module]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

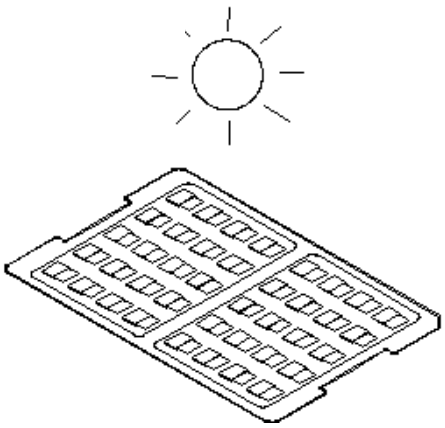
[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
(3) Keeping Method

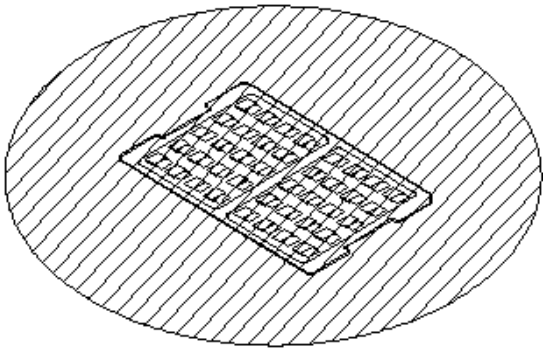
a. Don't keeping under the direct sunlight.

b. Keeping in the tray under the dark place.

DON'T



DO



(4) Do not operate or store the LCD module under outside of specified environmental conditions.
(5) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VDDI-GND) are low when LCD module is working, place the de-coupling capacitor nearby LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

(8) U/V glue (Liquid OCA) should not be attached on upper polarizer edge, when customer laminate cover glass and touch panel on LCD.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of active matrix 16,777,216 color LCD module.

Main color LCD module is controlled by Driver IC (NT35597 with 1/3 RAM).

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

This module is a color transmissive, high contrast, wide viewing angle and active matrix LCD module incorporating CG-Silicon TFT (Continuous Grain-Silicon Thin Film Transistor).

Construction: LCD panel, Driver (COG), FPC with electric components, LEDs, prism sheet, diffuser, light guide, reflector and plastic frame to fix them mechanically.

Outline: See page 36 (Fig.25 Outline dimensions)

Connection: Board-to-Board Plug Connector (JAE WP7B-P040VA1)

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

Rejection criteria shall be noted in Inspection Standard.

3. Mechanical Specification

Table 1

Item	Specifications	Unit	Remarks
Screen size	73.406 (2.89” type) Diagonal	mm	
Active area	51.84(H)X51.84(V)	mm	
Pixel format	1440(H)×1440(V)	Pixel	
	1 Pixel =R+G+B dots	-	
Pixel pitch	0.012 (H) x 0.036(V)	mm	
Pixel configuration	R,G,B vertical stripes	-	
Display mode	Normally Black	-	
LDC Driving method	DC Driving / 1H Z-Inversion	-	
Liquid Crystal Mode	New Mode2	-	
Number of colors	16,777,216	Colors	24 bits
Outline dimensions	54.24 X 59.02 X 1.365	mm	Note 3-1
Mass	7	g	

Note 3-1) The above-mentioned table indicates module sizes without some projections and FPC.

4. Pixel Configuration

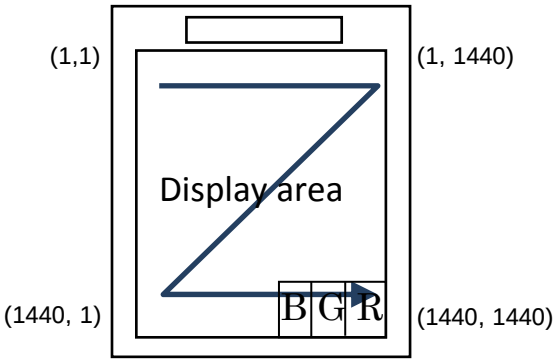


Fig.1

5. Input Terminal Names and Functions

Table 2

Pin No	Symbol	I/O	Description	Remarks
1	DSIA_D3_N	I	MIPI data3 negative signal of MIPI Port A	
2	DSIA_D3_P	I	MIPI data3 positive signal of MIPI Port A	
3	DSIA_D0_N	I/O	MIPI data0 negative signal of MIPI Port A	
4	DSIA_D0_P	I/O	MIPI data0 positive signal of MIPI Port A	
5	DSIA_CLK_N	I	MIPI clock negative signal of MIPI Port A	
6	DSIA_CLK_P	I	MIPI clock positive signal of MIPI Port A	
7	DSIA_D1_N	I	MIPI data1 negative signal of MIPI Port A	
8	DSIA_D1_P	I	MIPI data1 positive signal of MIPI Port A	
9	DSIA_D2_N	I	MIPI data2 negative signal of MIPI Port A	
10	DSIA_D2_P	I	MIPI data2 positive signal of MIPI Port A	
11	DSIB_D2_P	I	MIPI data2 positive signal of MIPI Port B	
12	DSIB_D2_N	I	MIPI data2 negative signal of MIPI Port B	
13	DSIB_D1_P	I	MIPI data1 positive signal of MIPI Port B	
14	DSIB_D1_N	I	MIPI data1 negative signal of MIPI Port B	
15	DSIB_CLK_P	I	MIPI clock positive signal of MIPI Port B	
16	DSIB_CLK_N	I	MIPI clock negative signal of MIPI Port B	
17	DSIB_D0_P	I/O	MIPI data0 positive signal of MIPI Port B	
18	DSIB_D0_N	I/O	MIPI data0 negative signal of MIPI Port B	
19	DSIB_D3_P	I	MIPI data3 positive signal of MIPI Port B	
20	DSIB_D3_N	I	MIPI data3 negative signal of MIPI Port B	
21	EN1PORT	I	EN1PORT is used for enable or disable MIPI dual port	“H” single port
22	AVDD	-	Power supply for analog	
23	VDDI	-	Power supply for I/O	
24	VDDI	-	Power supply for I/O	
25	EXCK	I	External Clock (not used)	GND
26	GND	-	Ground	
27	GND	-	Ground	
28	GND	-	Ground	
29	RESX	I	Device reset signal	“L” Active
30	FTE	O	Frame head pulse signal (not used)	Open
31	Sync	O	Synchronizing signal (not used)	Open
32	LEDPWM	O	Backlight LED driver PWM (if not used, “floating”)	
33	AGND	-	Ground	
34	AGND	-	Ground	-
35	AGND	-	Ground	I
36	AVEE	-	Power supply for analog	I
37	LED_CA1		LED back light power negative1	I
38	LED_CA2		LED back light power negative2	I
39	LED_AN1		LED back light power positive1	-
40	LED_AN2		LED back light power positive2	-

Fitting connector: JAE WP7B-S040VA1 (Board-to-Board Receptacle)

Pin layout: See Outline dimensions. (P.35)

Recommended outside circuit:

<MIPI DSI (Single Port)>

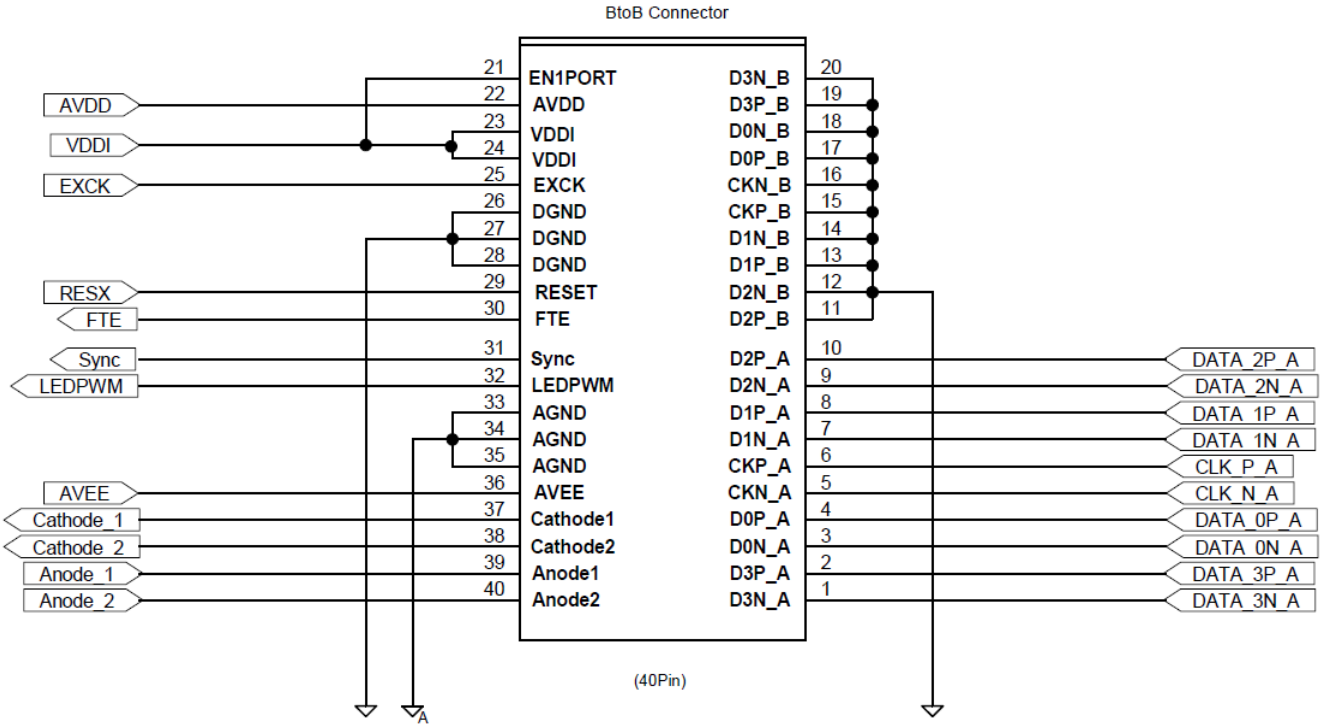


Fig.2

<MIPI DSI (Dual Port)>

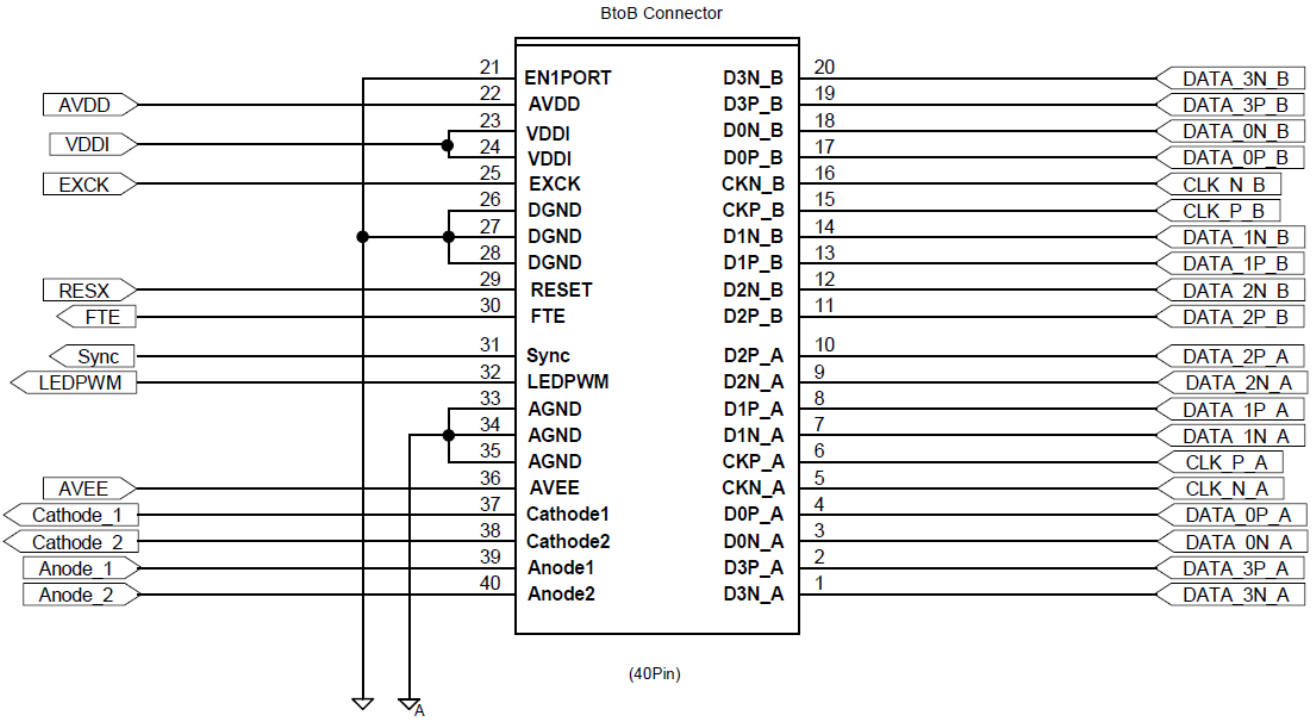


Fig.3

6.Absolute Maximum Ratings

Table3 GND=0V

Parameter	Symbol	Conditions	Rated value	Unit	Remarks
Driver IC (Positive Analog) Power Supply Voltage	AVDD	Ta=+25°C	-0.3 to +6.5	V	Note6-1
Driver IC (Negative Analog) Power Supply Voltage	AVEE	Ta=+25°C	+0.3 to -6.5	V	Note6-1
Driver IC (Digital) Power Supply Voltage	VDDI	Ta=+25°C	-0.3 to +5.5	V	Note6-1
Temperature for storage	Tstg	-	-30 to +70	°C	Note6-2
Temperature for operation	Topr	-	-20 to +60	°C	Note6-2
LED Input electric current	ILED	Ta=+25°C	25	mA	Note6-3

Note6-1) Voltage applied to GND pins. GND pin conditions are based on all the same voltage (0V).
Always connect all GND externally and use at the same voltage.

Note6-2)Humidity: 95%RHMax.(at Ta≤40°C). Maximum wet-bulb temperature is less than 39°C (at Ta>40°C). Condensation of dew must be avoided.

Note6-3) Ambient temperature and the maximum input are fulfilling the following operating conditions.

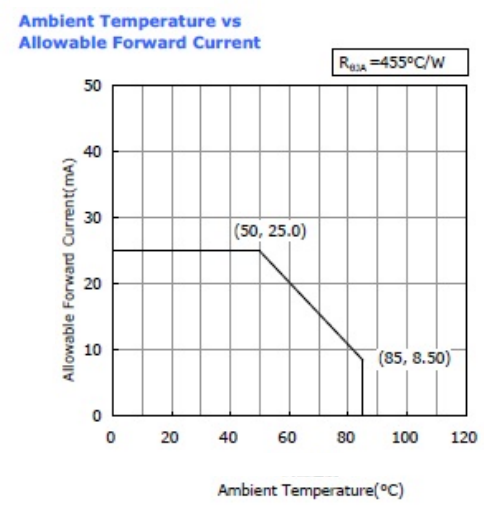


Fig.4

7. Electrical Specifications

7-1. TFT-LCD Panel Driving Section

Table4 Ta=+25°C, GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Driver IC(Digital) Power Supply Voltage	VDDI	1.70	1.80	1.9	V	Note7-1
Driver IC(Positive Analog) Power Supply Voltage	AVDD	5.3	5.5	5.7	V	Note7-1
Driver IC(Negative Analog) Power Supply Voltage	AVEE	-5.7	-5.5	-5.3	V	Note7-1
Input voltage (Low)	V_{IL}	0	-	0.3 VDDI	V	Note7-2
Input voltage (High)	V_{IH}	0.7 VDDI	-	VDDI	V	Note7-2
Input current (Low)	I_{IL}	-10	-	-	μA	
Input current (High)	I_{IH}	-	-	10	μA	
Output voltage (Low)	V_{OL}	0	-	0.2 VDDI	V	I_{OL}=+0.1mA
Output voltage (High)	V_{OH}	0.8 VDDI	-	VDDI	V	I_{OH}=-0.1mA
Current consumption Video mode with RAM 2port(SDC)	I_{VDDI4}	TBD	TBD	TBD	mA	
	I_{AVDD4}	TBD	TBD	TBD	mA	
	I_{AVEE4}	TBD	TBD	TBD	mA	

Note7-1) Include Ripple Noise

Note7-2) Applied overshoot

7-2. Back Light Driving Section

Table5 Ta=+25°C,GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
LED Voltage	V_{LED}	-	2.9	3.2	V	per unit
LED Current	I_{LED}	-	11	20	mA	
Power Consumption	W_{LED}	-	255.2	-	mW	
LED Quantity		8			pcs	

8. Timing characteristics of input signals

8-1. MIPI DC/AC Characteristics

<DC characteristics>

Table6

Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VDDAM	Power supply voltage for MIPI RX	1.65	1.8	1.95	V
VP_HSSI	High speed / Low power mode operating voltage		1.2		V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40			mV
VIHHS	Single-ended input high voltage			460	mV
VCMRXDC	Common-mode voltage	70		330	mV
ZID	Differential input impedance	80	100	125	ohm
|VOD|	HS transmit differential voltage (VOD=VDP-VDN)	140	200	250	mV
V_{IDTH}	Different input high threshold			70	mV
V_{IDTL}	Different input low threshold	-70			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50		1350	mV
VGNDSH	Ground shift	-50		50	mV
VIL	Logic 0 input threshold	0.0		550	mV
VIH	Logic 1 input threshold	880		VDDAM	mV
VHYST	Input hysteresis	25			mV
VOL	Output low level	-50		50	mV
VOH	Output high level	1.1	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	80	100	125	ohm
VIHCD,MAX	Logic 0 contention threshold	0.0		200	mV
VILCD,MIN	Logic 1 contention threshold	450		VDDAM	mV

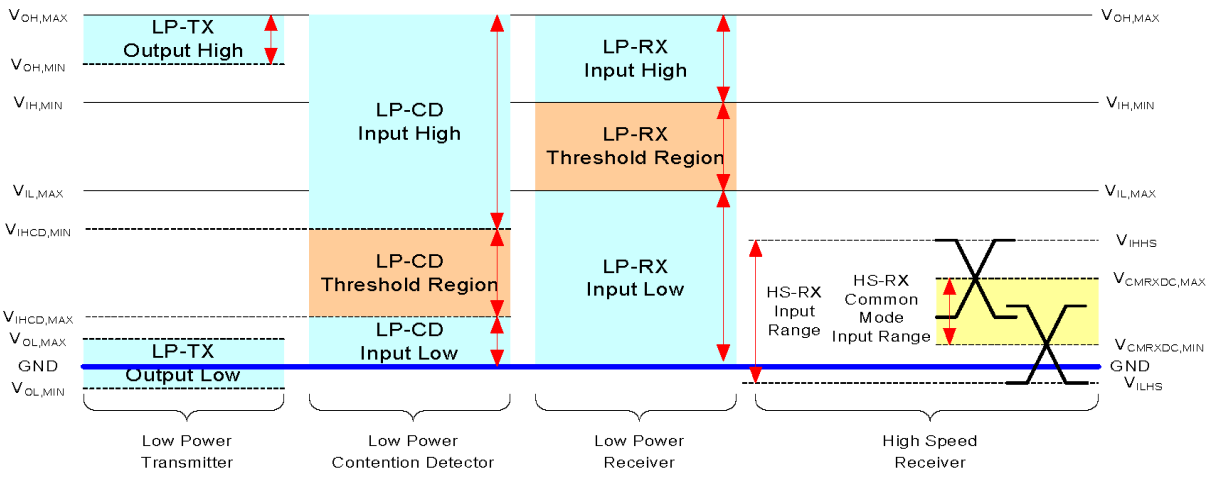


Fig.5

<AC Characteristics>

High Speed Data Transmission: Data-Clock Timing

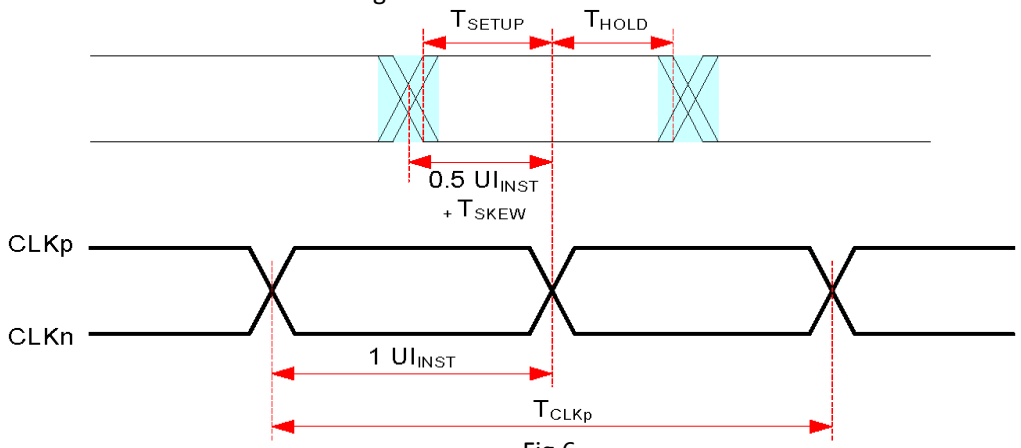


Fig.6

Table7

Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2,10
Data to Clock Skew [measured at tansmitter]	T_{SKEW}[TX]	-0.15		0.15	UI_{INST}	3
		-0.2		0.2	UI_{INST}	4
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	0.15		0.15	UI_{INST}	5
		0.2		0.2	UI_{INST}	6
Data to Clock Hold Time [measured at reciever]	T_{HOLD}[RX]	0.15		0.15	UI_{INST}	5
		0.2		0.2	UI_{INST}	6
20% - 80% rise time and fall time	t_R / t_F	100			ps	9
				0.3	UI_{INST}	7
				0.35	UI_{INST}	8

Note:

1. This value corresponds to a minimum 80 Mbps data rate.

2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.

3. Total silicon and package delay budget of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

4. Total silicon and package delay budget of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

5. Total setup and hole window for receiver of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

6. Total setup and hole window for receiver of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

7. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).

8. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

9. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

10. For MIPI speed limitation:

[1] Per lane bandwidth is 1Gbps,

[2] Total Bit Rate: 4Gbps for 8-8-8; 3Gbps for 6-6-6; and 2.67Gbps for5-6-5.

LP Transmission AC Specification

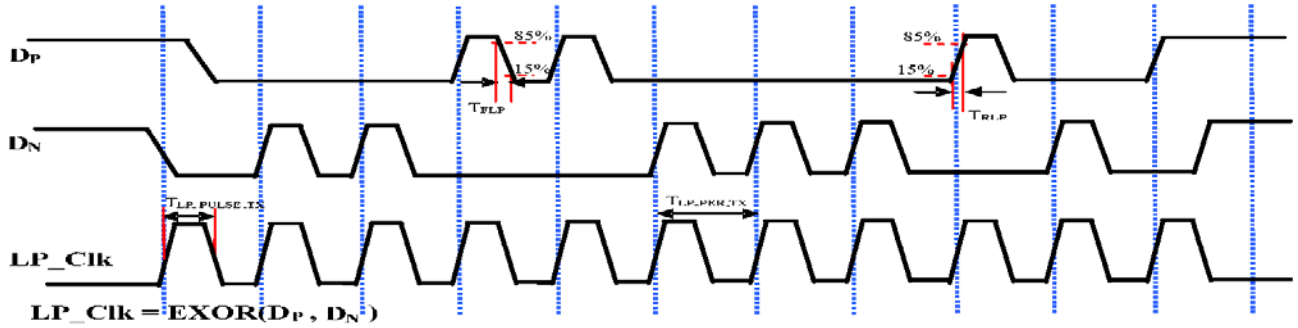


Fig.7

Table8

Parameter		Symbol	Min	Typ	Max	Units	Notes
15%-85% rise time and fall time		T_{RLP} / T_{FLP}			25	ns	1
30%-85% rise time and fall time		T_{REOT}			35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	$T_{LP-PULSE-TX}$	40			ns	4
	All other pulses		20			ns	4
Period of the LP exclusive-OR clock		$T_{LP-PER-TX}$	90			ns	
Slew Rate@ C_{LOAD} = 0pF		$\delta V/\delta t_{SR}$	30		500	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 5pF			30		200	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 20pF			30		150	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 70pF			30		100	mV/ns	1,2,3,7
Load Capacitance		C_{LOAD}			70	pF	1

Note:

1. *CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.*
2. *When the output voltage is between 15% and below 85% of the fully settled LP signal levels.*
3. *Measured as average across any 50 mV segment of the output signal transition.*
4. *This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.*
5. *The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*
6. *With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.*
7. *This value represents a corner point in a piecewise linear curve as bellowed.*

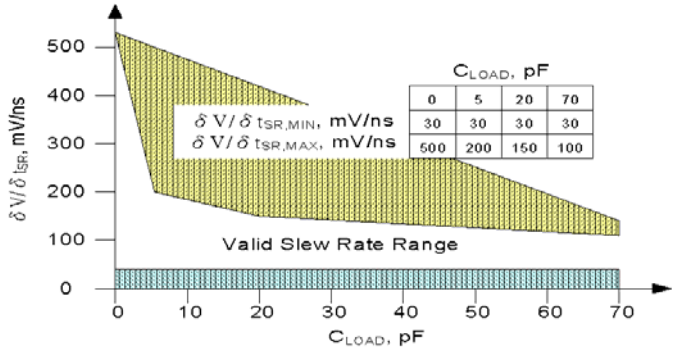


Fig.8

High-Speed Data Transmission in Bursts

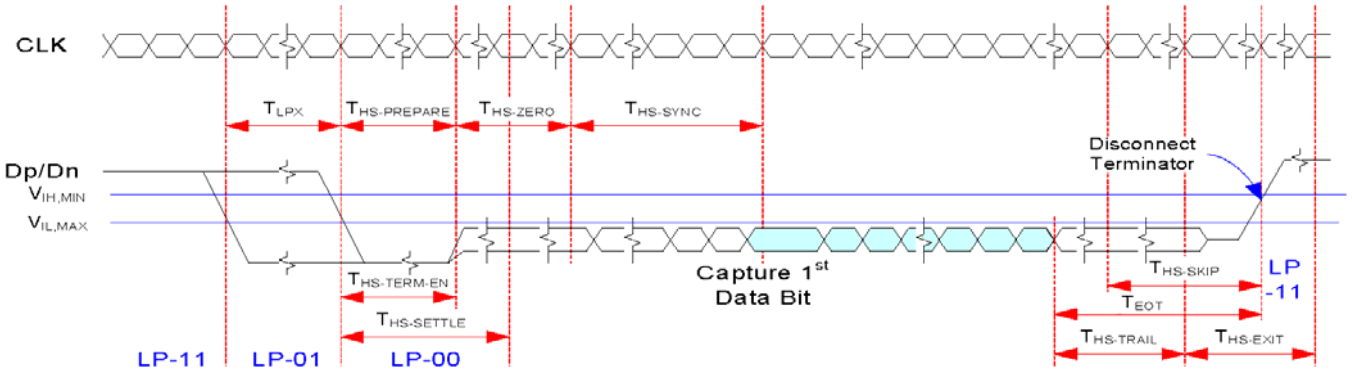


Fig.9

Table9

Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Note:
1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2: UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.
3: TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

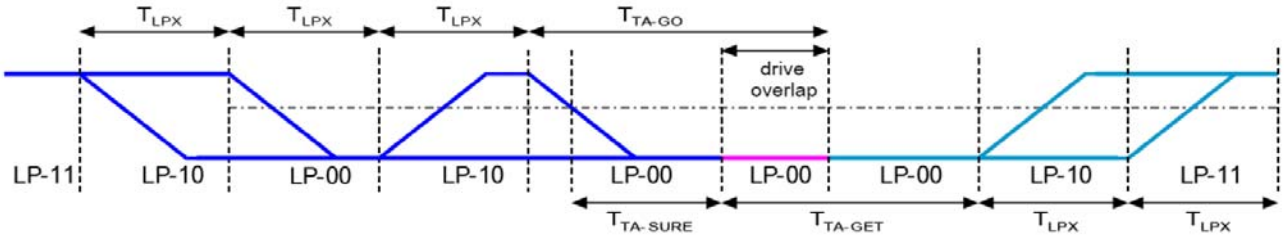


Fig.10

Table10

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode

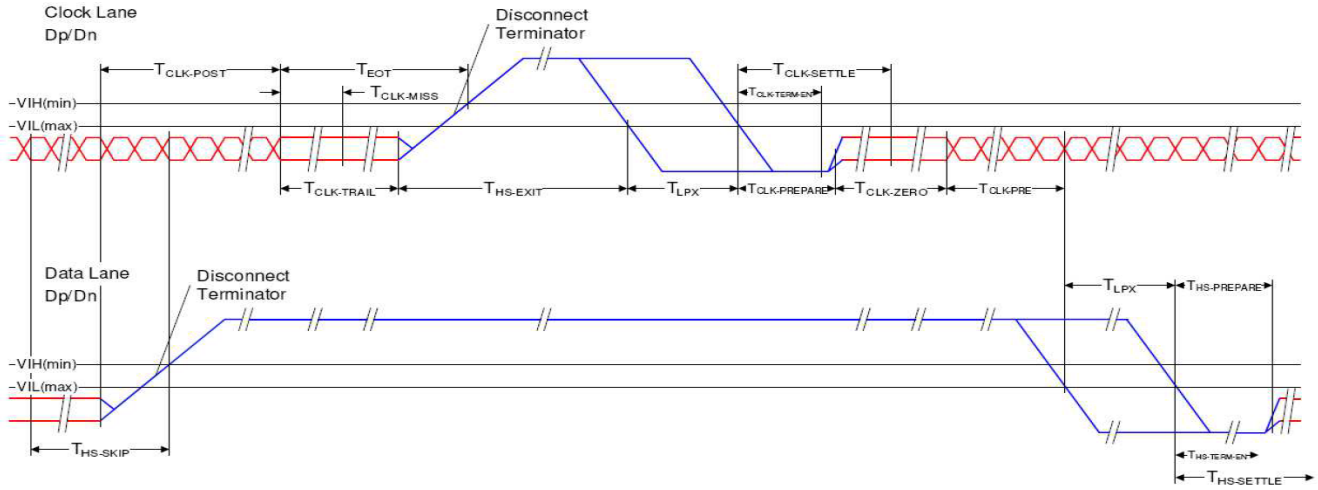


Fig.11

Table11

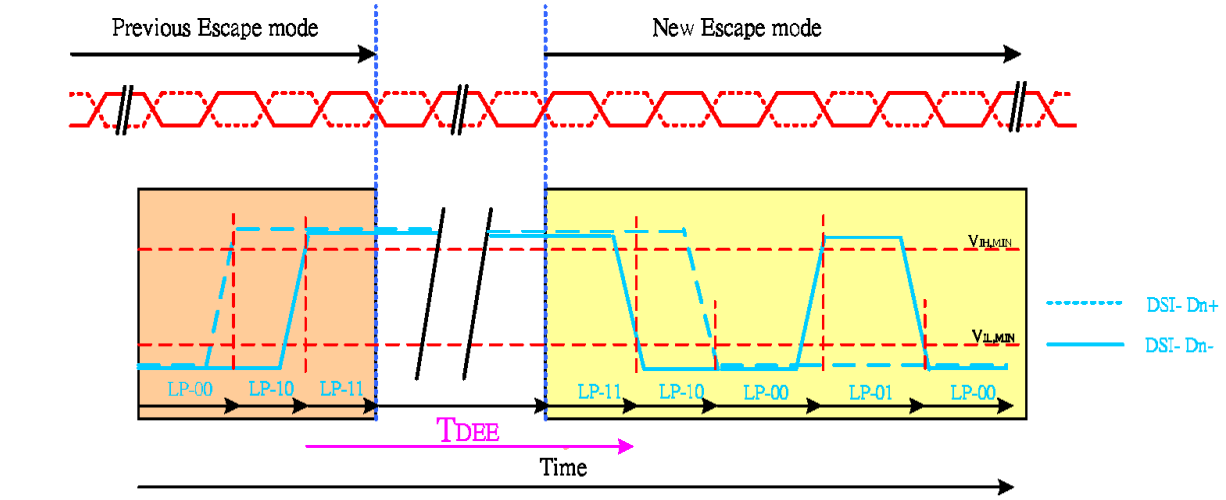
Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode **(RM=0)**	$T_{CLK-POST}$	**60ns+ 132UI (note1)**			ns
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode **(RM=1, Compression_Method[1:0]= 0h)**	$T_{CLK-POST}$	**60ns + 420UI (note1)**			ns
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode **(RM=1, Compression_Method[1:0]= 1/2/3/4h)**	$T_{CLK-POST}$	**60ns + 132UI (note1)**			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

Note1. This values need to correspond with a minimum 500 MHz data rate".

LP11 timing request between data transformation

When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP – LP, LP – HS, HS – LP, HS – HS, BTA – BTA, LP – BTA, BTA – LP, HS – BTA, and BTA – HS. This rule is suitable for short or long packet between TX and RX data transmission.

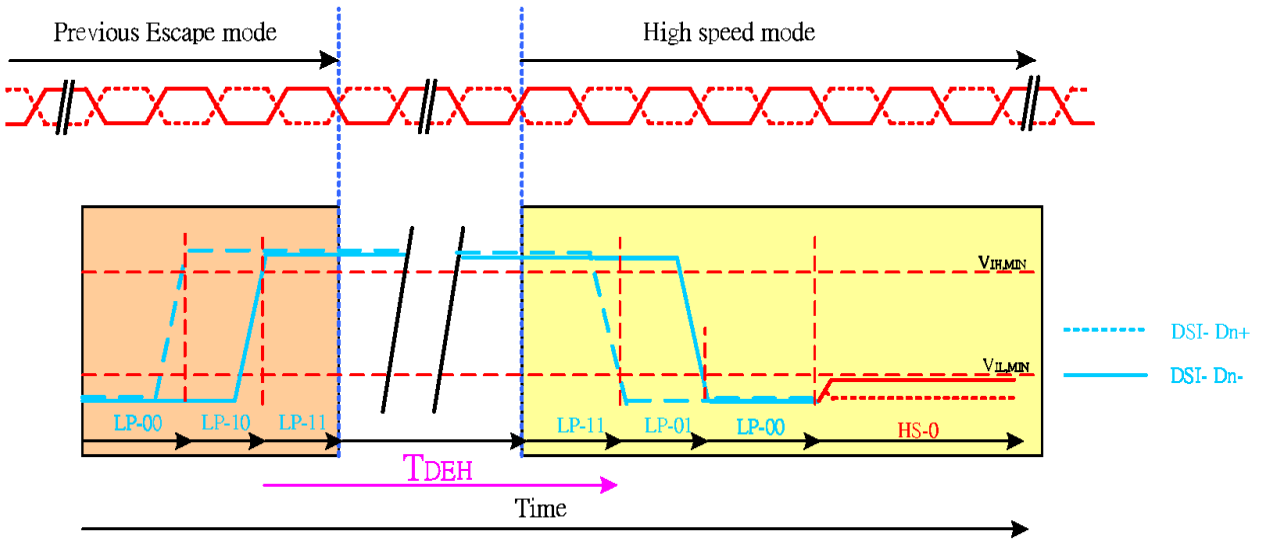
(1) Timing between LP – LP command



Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the new Escape Mode Entry	T_{DEE}	100			ns

Fig.12

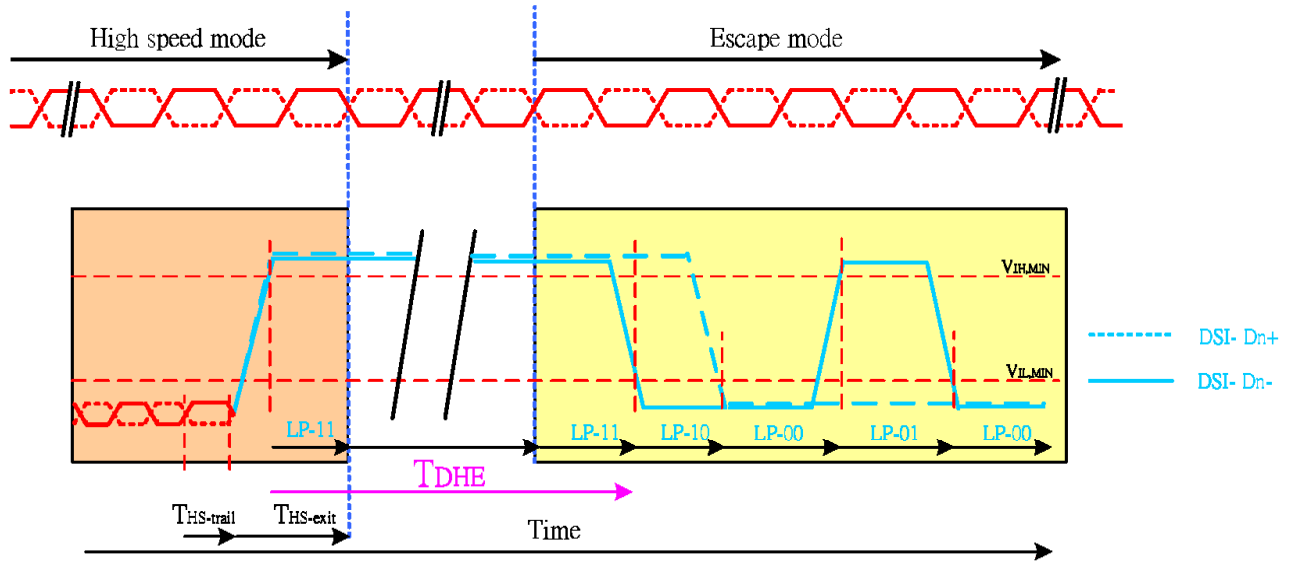
(2)Timing between LP – HS command



Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Entering High Speed Mode	T_{DEH}	Max(100,32UI)			ns

Fig.13

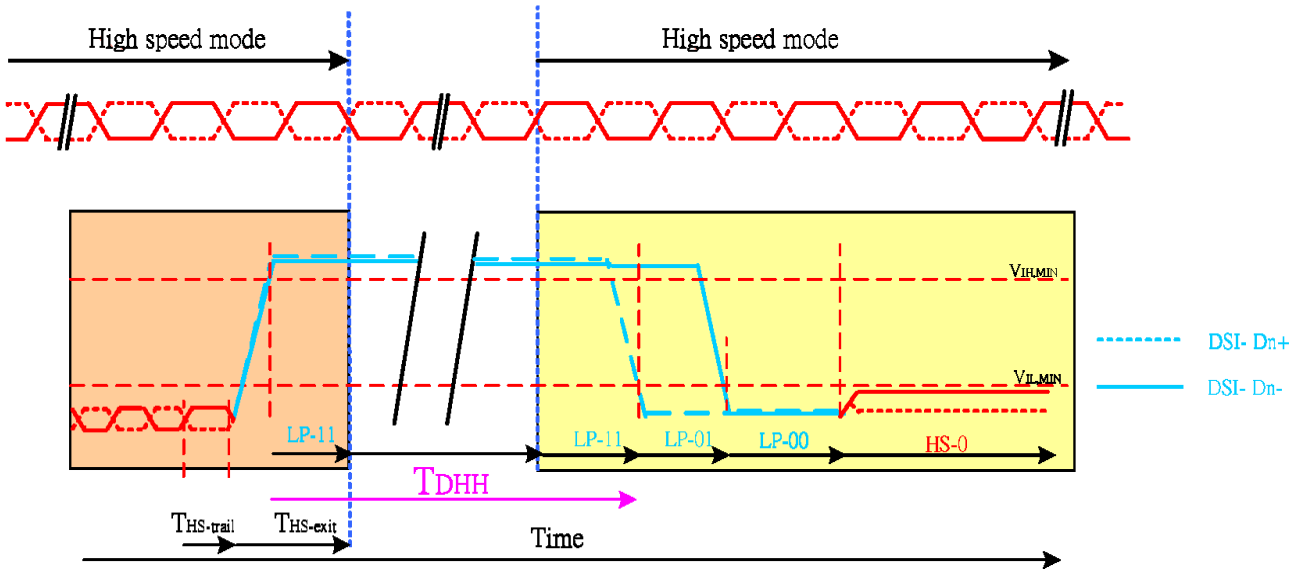
(3)Timing between HS – LP command



Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Escape Mode Entry	T_{DHE}	Max(100,32UI)			ns

Fig.14

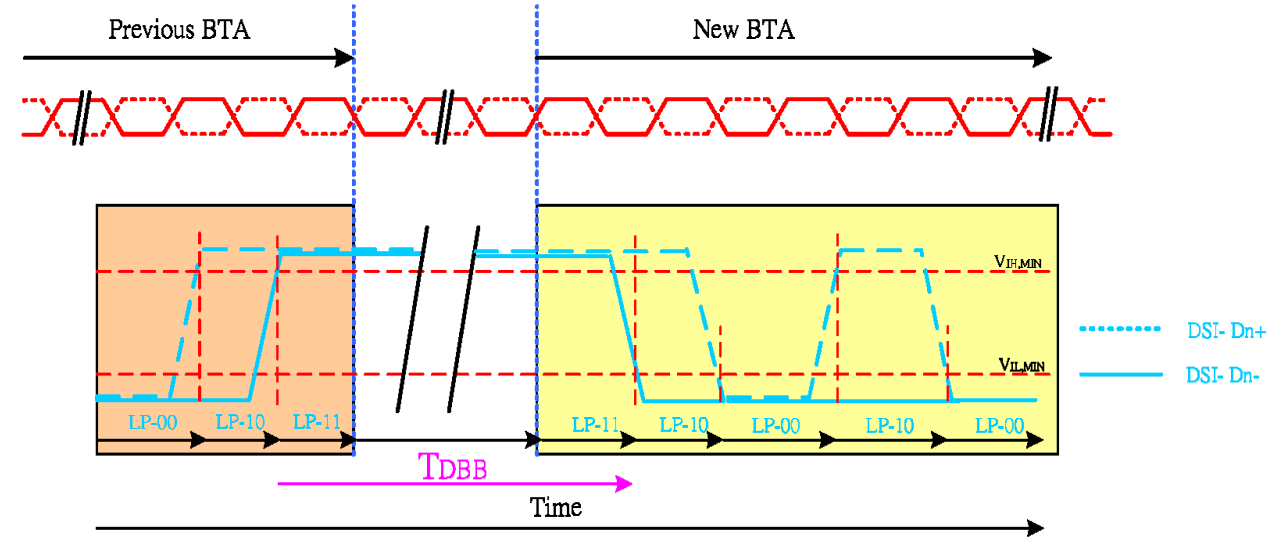
(4)Timing between HS –HS command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DHH}	Max(100,32UI)			ns

Fig.15

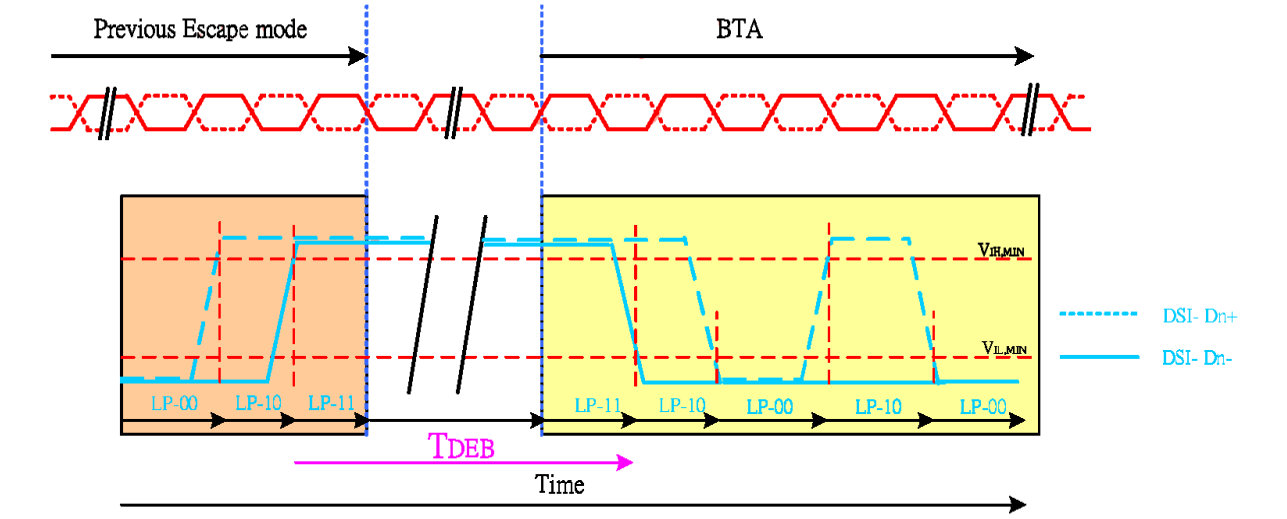
(5)Timing between BTA – BTA command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the new BTA	T_{DBB}	100			ns

Fig.16

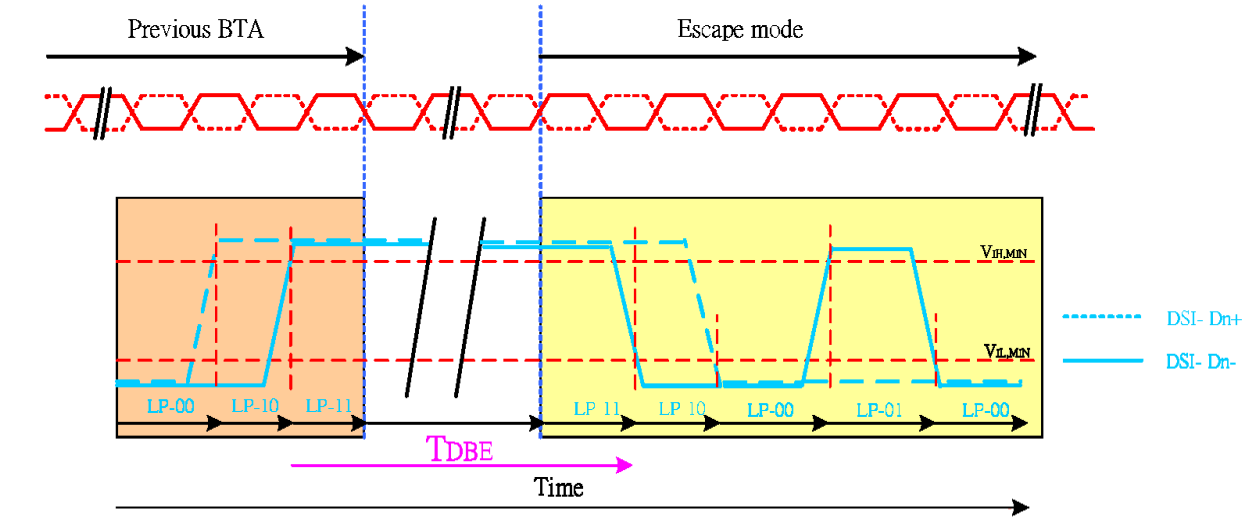
(6)Timing between LP– BTA command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DEB}	100			ns

Fig.17

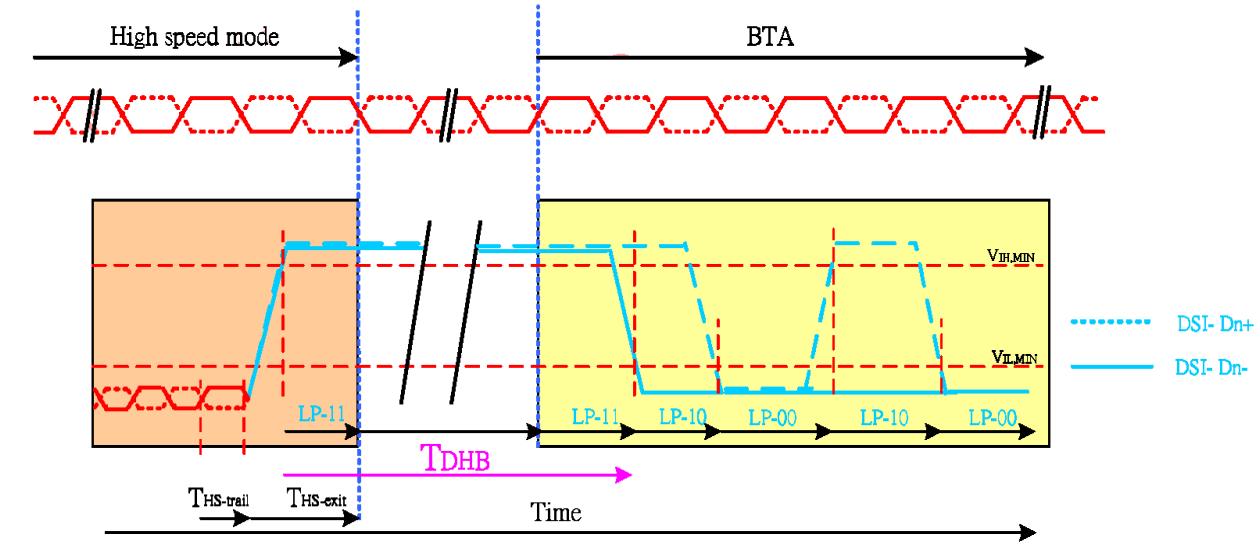
(7)Timing between BTA – LP command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Escape Mode Entry	T_{DBE}	100			ns

Fig.18

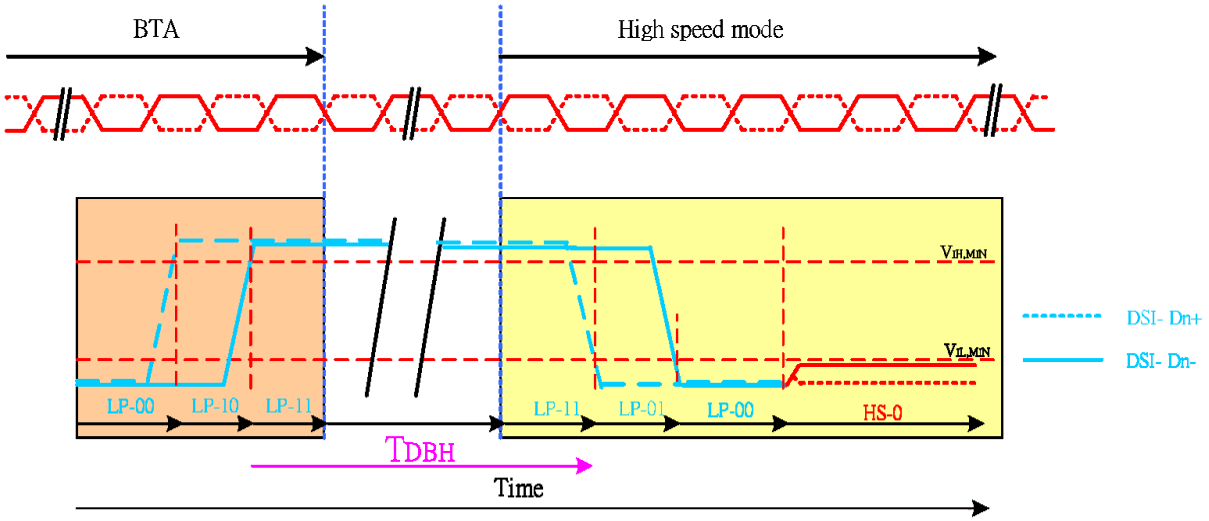
(8)Timing between HS – BTA command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DHB}	Max(100,32UI)			ns

Fig.19

(9)Timing between BTA – HS command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DBH}	Max(100,32UI)			ns

Fig.20

8-2 Reset Timing Characteristics

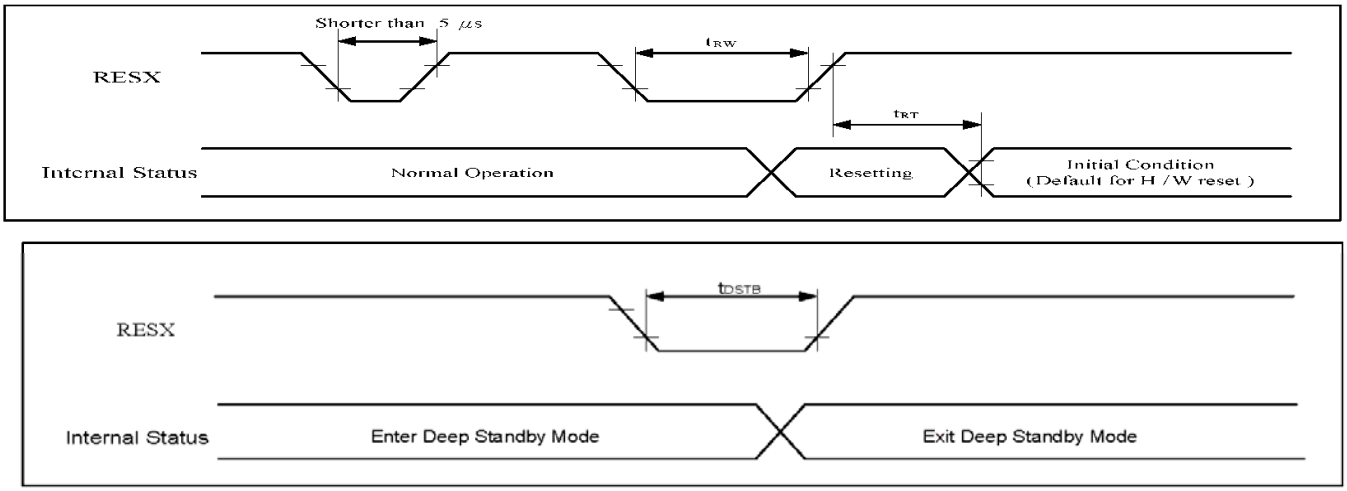


Fig.21

Table12

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	t_{RW}	Reset pulse duration	10(Note)	-	us
	t_{RT}	Reset cancel	-	10(Note)	ms
			-	120(Note)	ms
	tDSTB	Reset pulse duration	3	-	ms

Note :

-The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 10 ms after a rising edge of RESX.

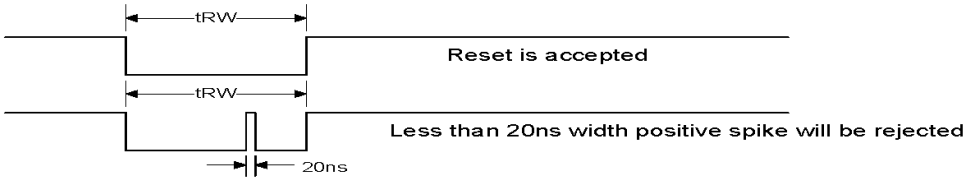
-Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :

Table13

RESX	Pulse Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

-During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-Spike Rejection also applies during a valid reset pulse as shown below :



-When Reset applied during Sleep-In Mode.

-When Reset applied during Sleep-Out Mode.

-It is necessary to wait 10ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

8-3 Display timing

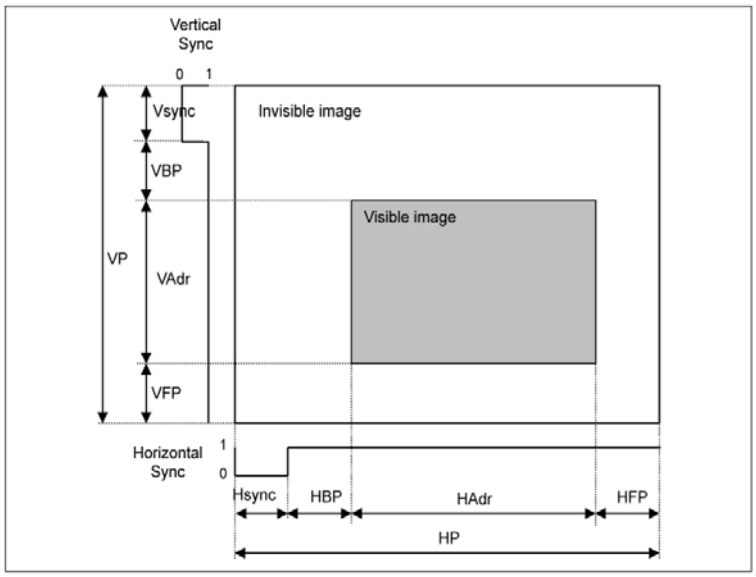


Fig.22

<SDC Display timing>

Table14 I/F:MIPI DSI 8lane no compression, Dots Size:1440xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		100		Pixel
Horizontal active area (HAdr)		1440		Pixel
Horizontal front porch(HFP)		154		Pixel
Vertical low pulse width(VS)		1		H
Vertical front porch(VFP)		264		H
Vertical back porch(VBP)		7		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(87.3)	90.2	(92.7)	Hz
1H Time	(6.286)	6.476	(6.675)	us
DSI DATA rate	(761.3)	(784.8)	(808.3)	Mbps/Lane

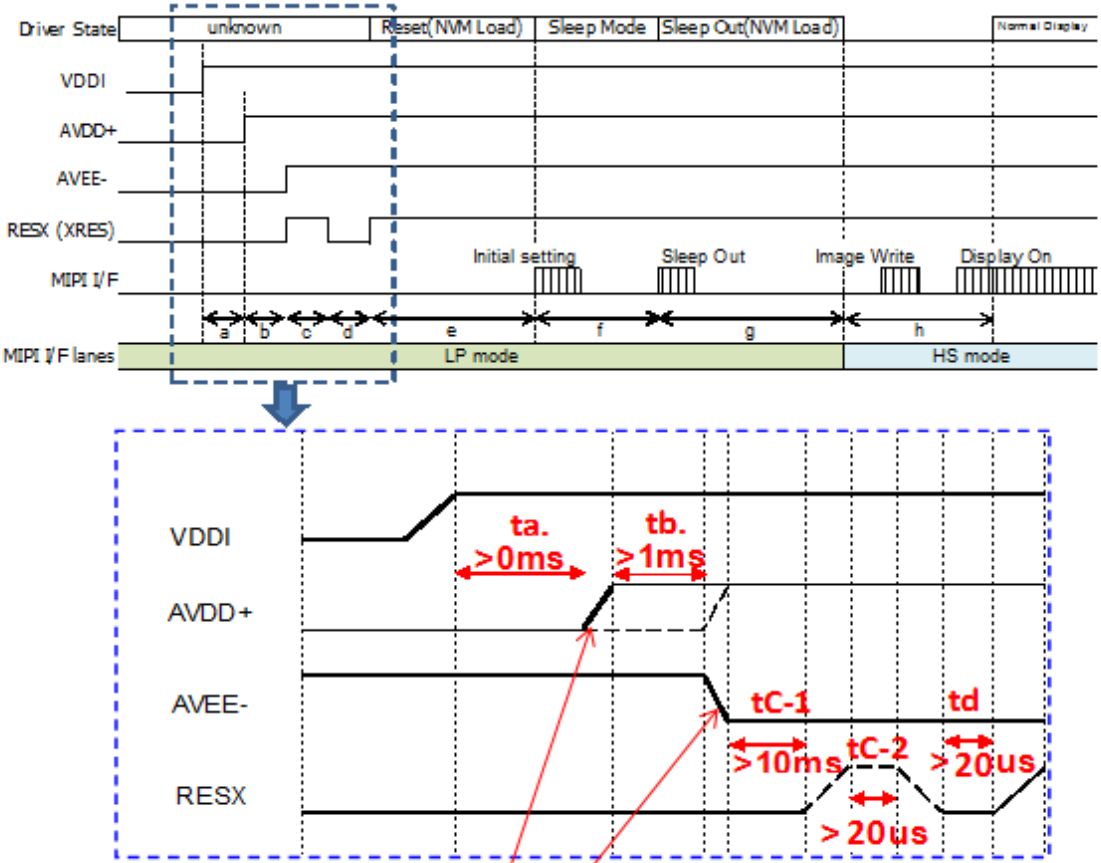
<VESA DSC Display timing>

Table15 I/F:MIPI DSI 4lane with compression, Dots Size:480xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		46		Pixel
Horizontal active area (HAdr)		480		Pixel
Horizontal front porch(HFP)		100		Pixel
Vertical low pulse width(VS)		1		H
Vertical front porch(VFP)		264		H
Vertical back porch(VBP)		7		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(87.3)	90.2	(92.7)	Hz
1H Time	(6.286)	6.476	(6.675)	us
DSI DATA rate	(562.6)	(580.0)	(597.4)	Mbps/Lane

9. Power Sequence

9-1 Power on sequence



Note:With the destination of avoiding latch-up issue,

the AVDD/AVEE slope time should set >0.2ms

Fig.23

Table 17: Recommended Power On Sequence

Step	Address	Parameter	Data	DSI data type		Delay	Command	
1	Initial condition						XRES = L	
2	Power Supply IOVDD (Typ1.8V)						IOVDD ON	
3	Wait					Min.>0 ms	(a.)Wait until IOVDD power stable	a.
4	Power Supply AVDD+ (Typ5.8V)						AVDD+ ON	
5	Wait					Min.>1 ms	(b.)After wait until AVDD+ power stable(rising slope > 0.2ms)	b.
6	Power Supply AVDD- (Typ-5.8V)						AVDD- ON	
7	Wait					Min.10 ms	(c.)After Wait until AVDD- power stable(rising slope > 0.2ms)	c-1.
8	RESX High						XRES = H	
9	Wait					Min.20us		c-2.
10	RESX go Low						XRES = L	
11	Wait					Min.20us		d.
12	RESX go Hi						XRES = H	
13	Wait					Min.10 ms	[Automatic] NVM Auto load	e.
14							[Automatic] Sleep Mode On	
15								
16	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
17	[CMD1]0x11	-	-	DCS	05h		Sleep Out	g.
18	Wait					Min.100ms		
19							[Automatic]Sleep Mode Off	
20	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
21	Display data transfer						Image Write	
22	[CMD1]0x29	-	-	DCS	05h		Display On	
23	Wait					Min.40 ms		
24							[Automatic] Display On	
25	Backlight on							

9-2 Power off sequence

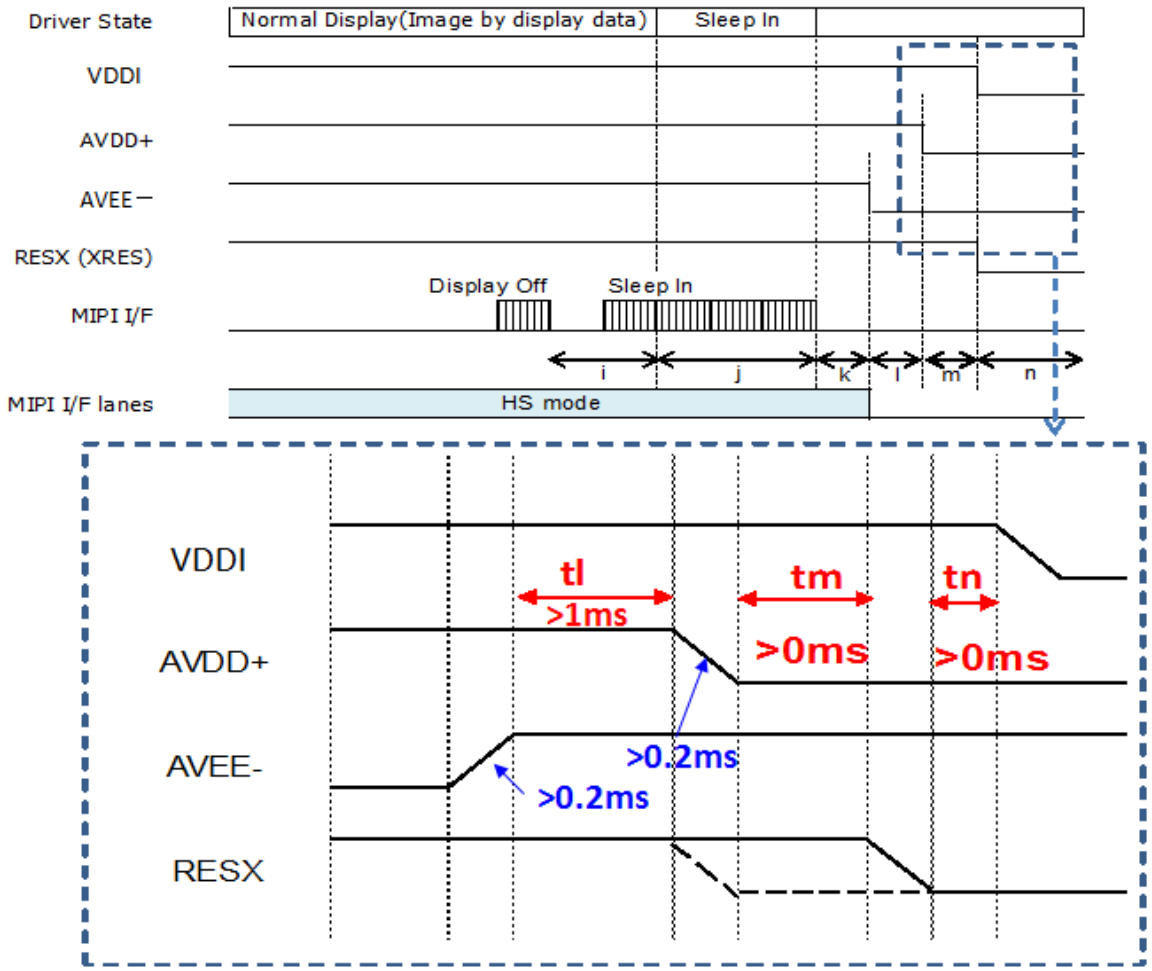


Fig.24

Table18: Recommended Power Off Sequence

Step	Address	Parameter	Data	DSI data type		Delay	Command	
1	28h	-	-	DCS	39h		Display Off	i
2	Wait					Min.1 frame		
3	10h	-	-	DCS	39h		Sleep In	j
4	Wait					Min. 4frame	Hsync/Vsync signals should be send after Sleep In command	
5							Mipi data transfer Stop	k
6	Wait					Min.0ms		
7	AVEE-(Typ-5.5V) OFF							l
8	Wait					Min.>1ms	Wait until AVDD- power stable(rising slope ＞0.2ms)	
9	AVDD+(Typ+5.5V) OFF							m
10	Wait					Min.>0ms	Wait until AVDD+ power stable(falling slope ＞0.2ms)	
11	RESX Low						XRES = L	n
12						Min.>0ms	Wait until RESX power stable	
13	VDDI OFF(Typ1.8V) OFF							

10. Input Signals, Basic Display Colors and Gray Scale of Each Color

Table 17

0: Low level voltage, 1: High level voltage

	Colors & Gray Scale	Gray Scale	Data signals																							
			R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
			LSB							MSB	LSB							MSB	LSB							MSB
Basic Color	Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	-	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	-	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	-	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	-	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	⇩	GS254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	GS255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								??								↓			
	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	⇩	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Each basic color can be displayed in 256 gray scales from 8 bit data signals. According to the combination of total 24 bit data signals, the 16,777,216-color display can be achieved on the screen.

11. Optical Characteristic

Table18 VDDI=1.8V, AVDD=5.5V, AVEE=-5.5V, ILED=11mA/pcs, Ta = 25℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	θ=0°	770	1100	-	-	Note11-1,2
Response Time	τr + τd	θ=0°	-	10	-	ms	Note11-3
White Chromaticity	x	θ=0°	0.240	0.290	0.340	-	
	y		0.265	0.315	0.365	-	
Red Chromaticity	x		0.615	0.665	0.715	-	
	y		0.260	0.310	0.360	-	
Green Chromaticity	x		0.210	0.260	0.310	-	
	y		0.545	0.595	0.645	-	
Blue Chromaticity	x		0.095	0.145	0.195	-	
	y		0.045	0.095	0.145	-	
Viewing Angle	θ11, θ12, θ21, θ22	CR>10	80	-	-	degree	Note11-1,2
Brightness	L	θ=0°	210	300	-	cd/m²	I_{LED}=11mA
Uniformity	U	θ=0°	70		-	%	Note11-4
NTSC Ratio	S	θ=0°	-	75	-	%	
Gamma	γ	θ=0°	1.8	2.2	2.6	-	
Flicker	F	θ=0°	-	-	30	%	Note11-5
Crosstalk	CT	θ=0°	-	-	5	%	Note11-6

*The measuring method of the optical characteristics is shown by the following figure.

*A measurement device is TOPCON luminance meter SR-3. (Measurement angle 1°)

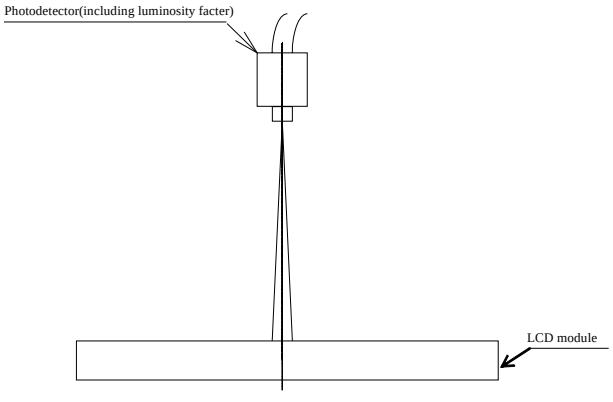


Fig.25

Note 11-1) Contrast / NTSC / GAMMA viewing angle is defined as follows.

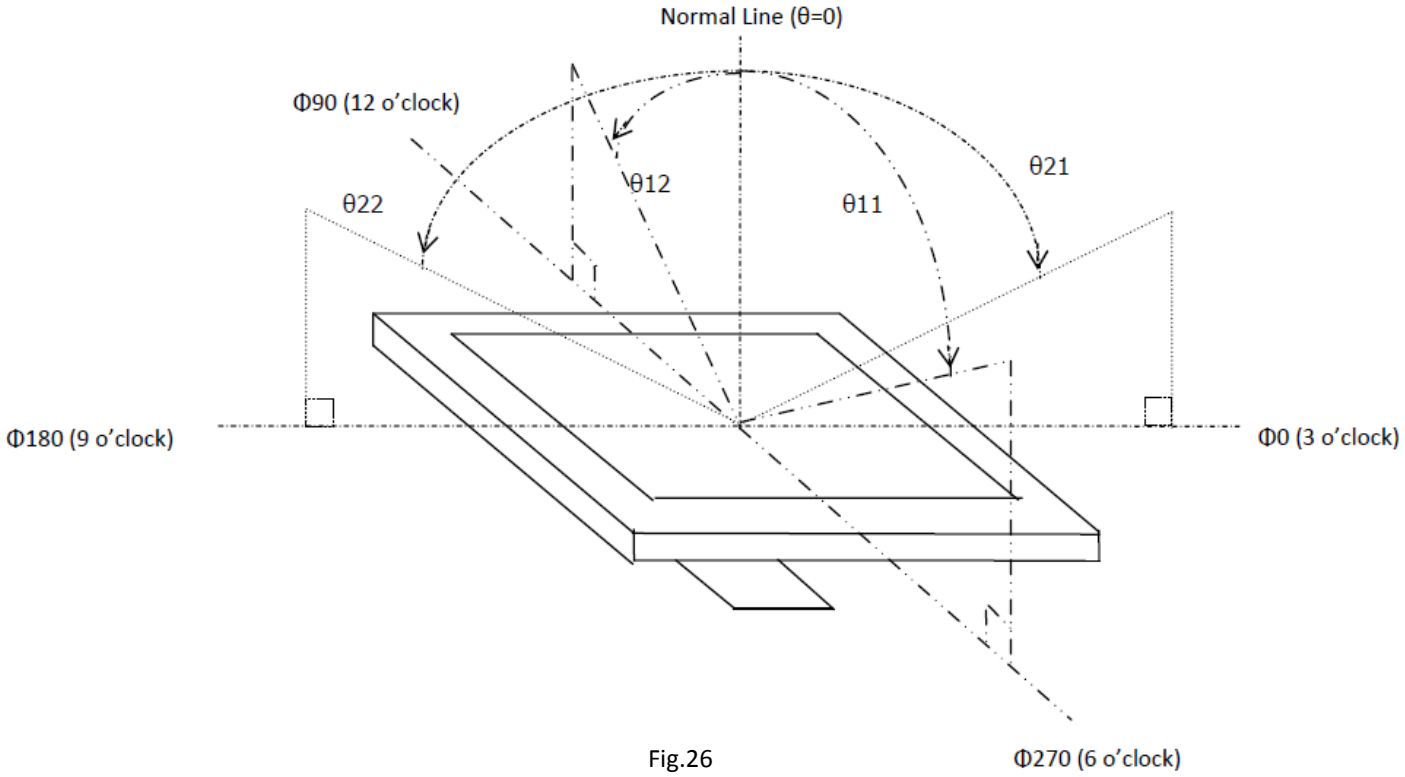


Fig.26

Note 11-2) Definition of contrast ratio:

The contrast ratio is defined as the follows:

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance(brightness) with all pixels white}}{\text{Luminance(brightness) with all pixels black}}$$

Note 11-3) Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”

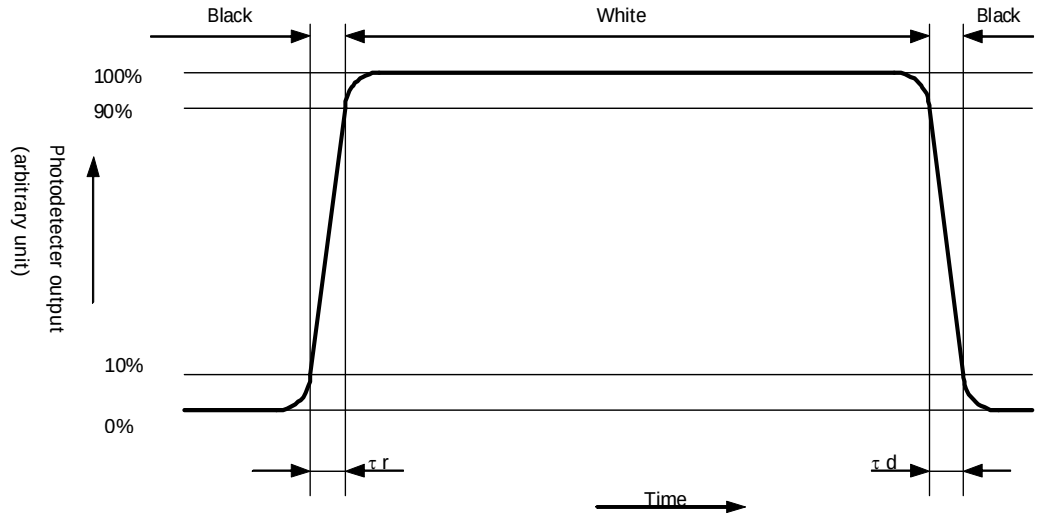

Black
White
Black
100%
90%
Photodetecter output
(arbitrary unit)
10%
0%
τ r
τ d
Time

Fig.27

Note 11-4) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

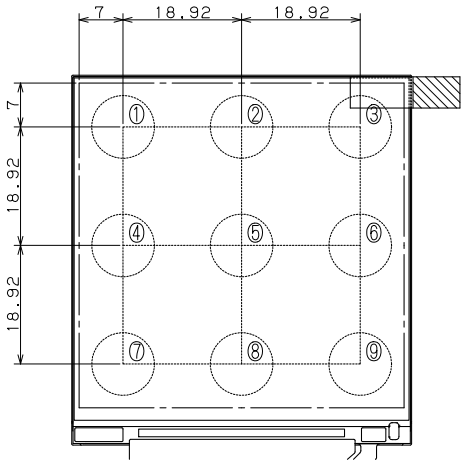


Fig.28

Note 11-5) Measuring systems: Konica-Minolta CA-310

- Temperature = 25°C (±3°C), Frame Frequency = 57Hz~63Hz, LED back-light: ON, Environment brightness < 150 lx
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.
- Measuring pattern Please refer to figure below.

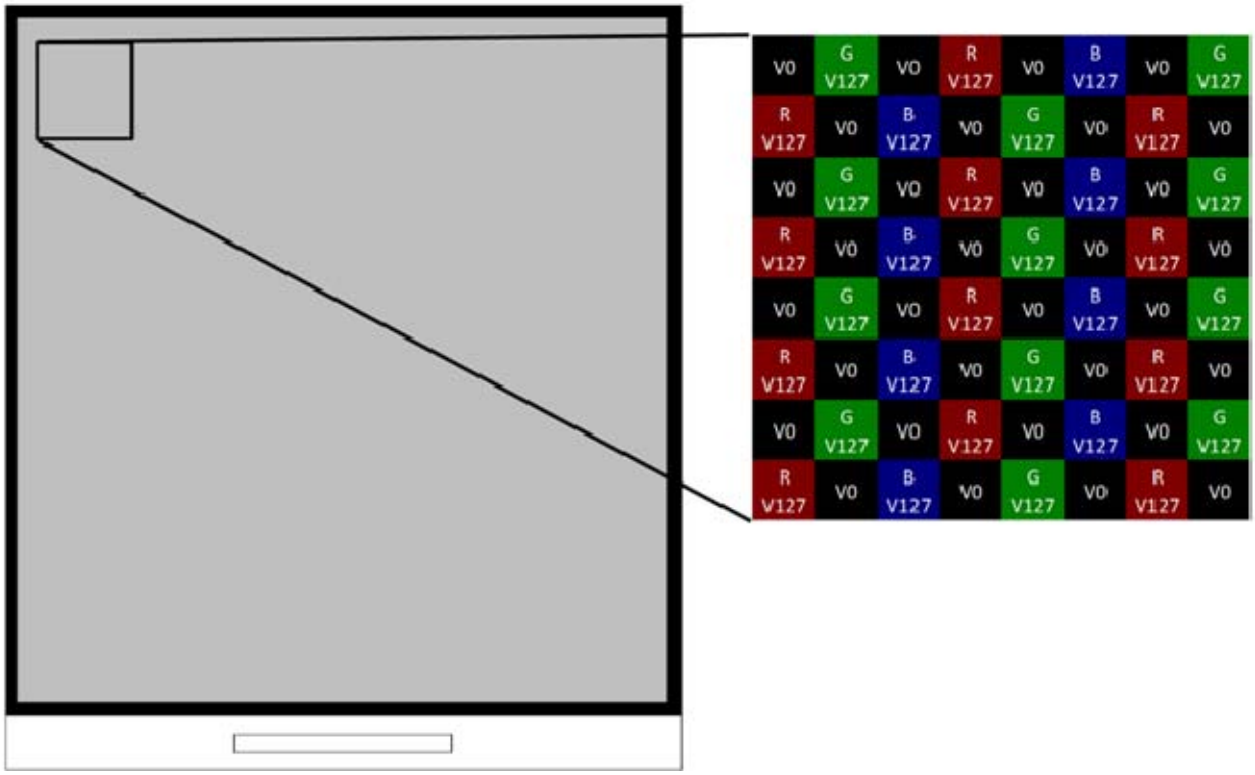


Fig.29

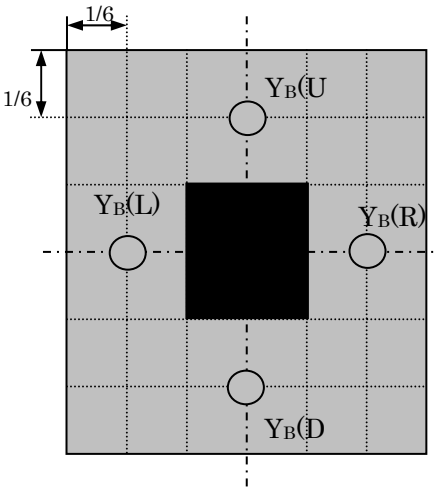
Note 11-6) Definition of Crosstalk

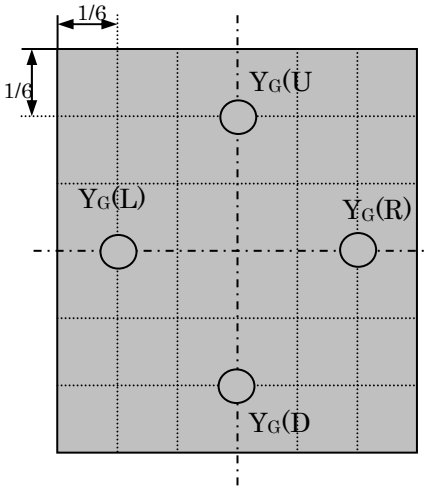
$$CT_B = \frac{|Y_B(x) - Y_G(x)|}{Y_G(x)} \times 100\,(\%)$$

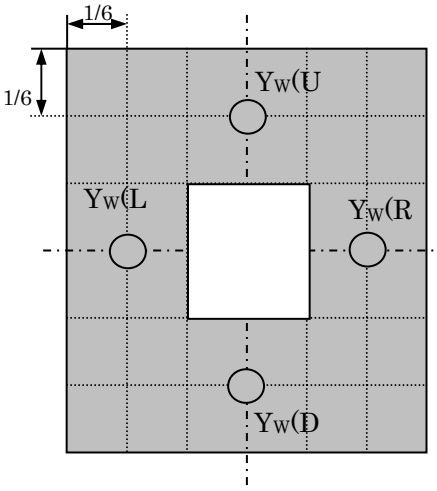
$$CT_W = \frac{|Y_W(x) - Y_G(x)|}{Y_G(x)} \times 100\,(\%)$$

x=U, D, L or R

Gray level=V128







12. Reliability

Table 19

No.	Test item	Conditions
1	High temperature storage test	Ta = +80°C, 200h
2	Low temperature storage test	Ta = -30°C, 200h
3	High temperature operation test	Ta = +70°C, 120h
4	Low temperature operation test	Ta = -20°C, 120h
5	High temperature and high humidity operation test	Ta = +50°C90%RH, 120h (No condensation)
6	Heat shock test	Ta = -20°C(30min) ~ 70°C(30min), 10 cycle
7	Electro static discharge test	±200V, 200pF(0Ω) to Terminals(Contact) (1 time for each terminals) None Operation
8	Packing Vibration test	Frequency: 5 to 50Hz (Round trip 3 minutes) Acceleration: 1G All Amplitude: 20 to 0.2mm Direction: Up/Down(60min), Left/Right(15min), Front/Back(15min) (3 Direction) Amplitude 20mm 0.2mm 20mm 0.2mm Frequency 5Hz 50Hz 5Hz 50Hz o———— o———— o ———— o |← 3 minutes →|
	Packing Drop test	Height: 75cm, Drop times: 10 Drop (1 Conner,3 Edges and 6 Faces)

Note 12-1) Ta = Ambient temperature

Note 12-2) Check items for other Test

In the standard condition, there shall be no practical problems that may affect the display function.

13. Indication of lot number

Attached location is shown in Fig. 30 Outline deimensions.

The lot number is shown on a label.

LS029B3SX01
F Y M D P XXXXX R

*Detail of S/N

LS029B3SX01	: Sharp model number	
F	: Factory code	/ STECH=E, Other=J
Y	: Manufacture year	/ 2015 = 5, 2016 = 6
M	: Manufacture month	/ January= 1, --- September= 9, October= A --- December=C
D	: Manufacture month	/ 1st= 1, --- 9th= 9, 10th= A --- 31th=X
P	:ID number of Printer	
XXXXX	: Serial number (5 digits)	/ 00001~99999
R	: Revision code	/ A, B, --------

14. Forwarding form

(a) Piling number of cartons: 8 deep

(b) Package quality in one cartons: 480 pcs

(c) Carton size: 580mm × 365mm × 279mm

(d) Total mass of 1 carton filled with full modules: approximately 9.3 kg

Condition for storage

Environment

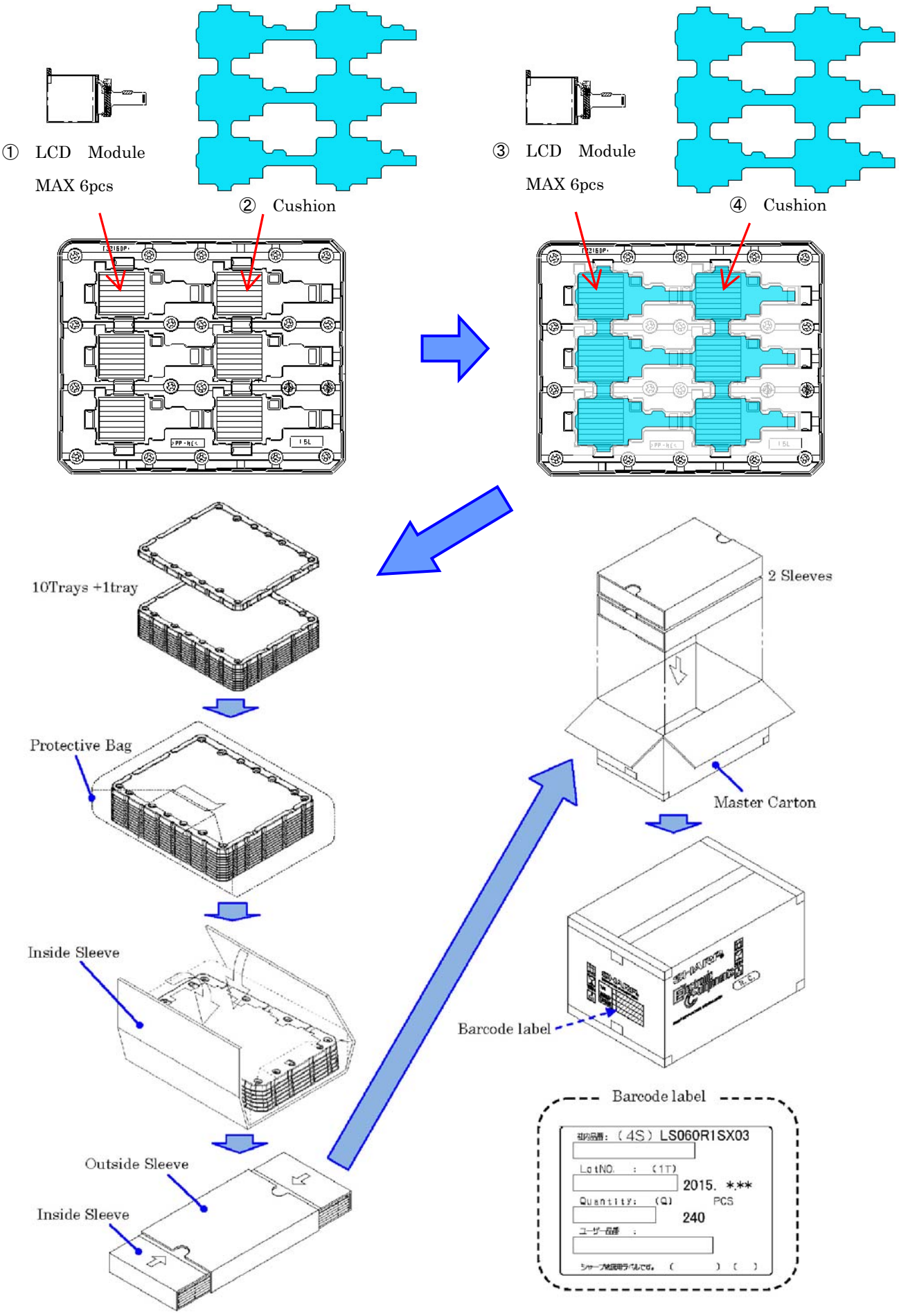
(1) Temperature: 0 to 40°C

(2) Humidity: 60%RH or less (at 40°C)

(3) Atmosphere: Harmful gas, such as acid or alkali which erodes electronic components and/or wires, must not be detected.

(4) Period: about 3 months

(5) Opening of the package: In order to prevent the LCD module from breakdown by electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as earth, etc.


① LCD Module
MAX 6pcs
② Cushion
③ LCD Module
MAX 6pcs
④ Cushion
10Trays +1tray
Protective Bag
Inside Sleeve
Outside Sleeve
Inside Sleeve
2 Sleeves
Master Carton
Barcode label
Barcode label
(4S) LS060R1SX03
LotNO. : (1T)
2015. *.**
Quantity: (Q) PCS
240

Outline dimensions

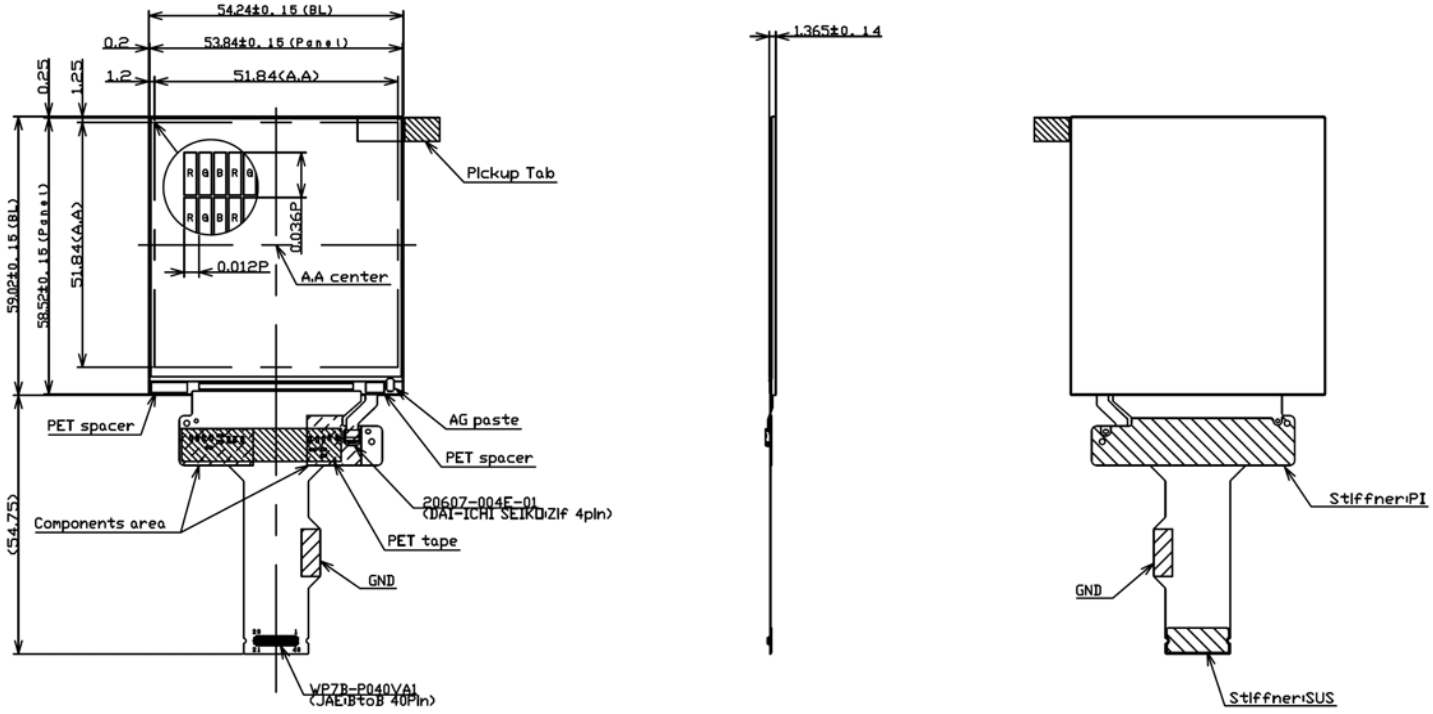


Fig.30

FPC Schematic

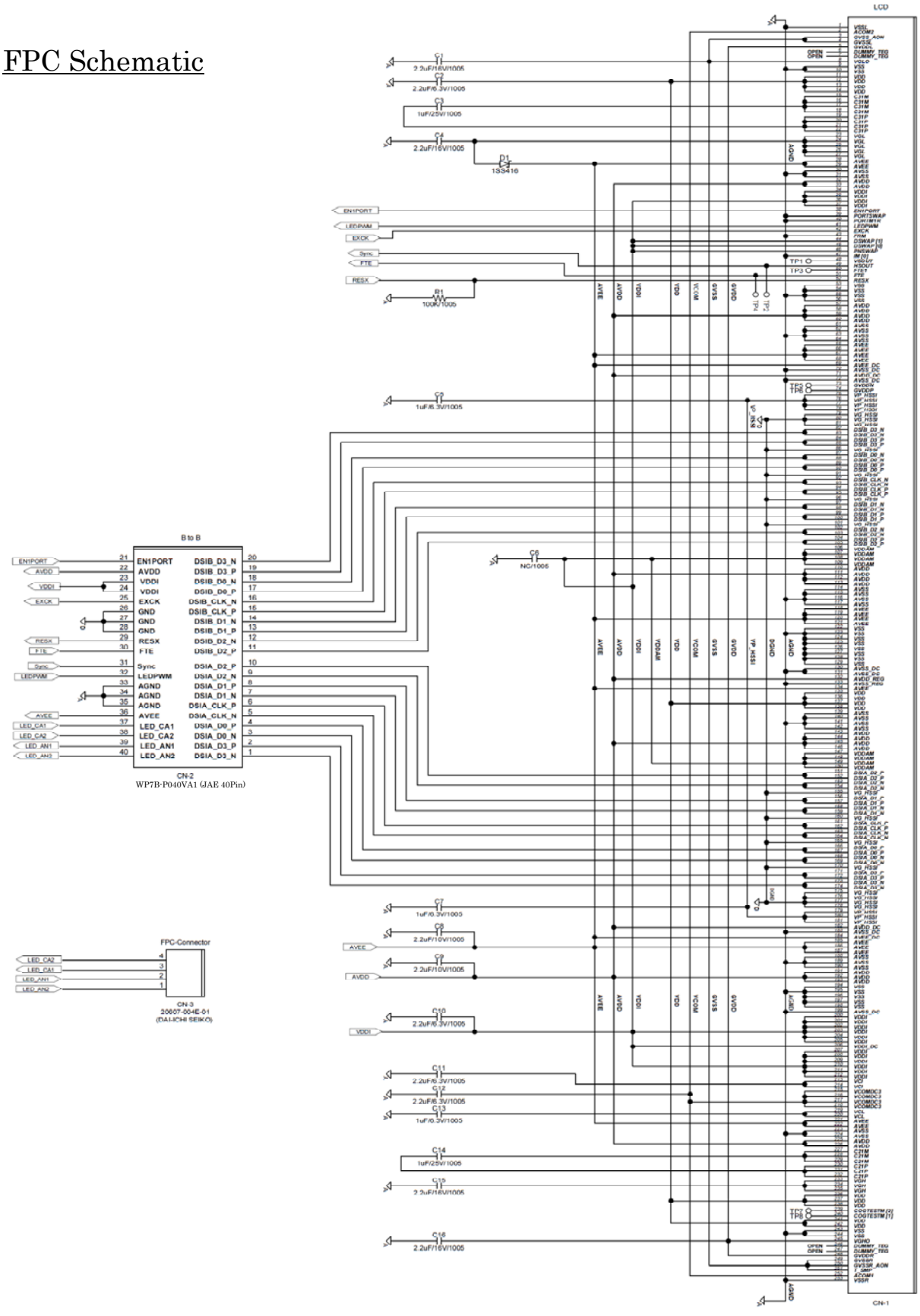


Fig.31