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		APPLICABLE DIVISION  DEVELOPMENT DEPARTMENT 1 BUSINESS UNIT 1 BUSINESS DIVISION 1 DISPLAY DEVICE COMPANY

DEVICE SPECIFICATION for  
 CGS Color LCD Module  
 (1440 × RGB × 1440 dots)  
  
 Model No.  
**LS029B3SX02**

CUSTOMER'S APPROVAL DATE

DATE \_\_\_\_\_

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### [For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not harm polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment.

There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the counter measure (electrostatic earth:  $1 \times 10^8 \Omega$ ) should be made.

④ Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤ Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥ Others

Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.

(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

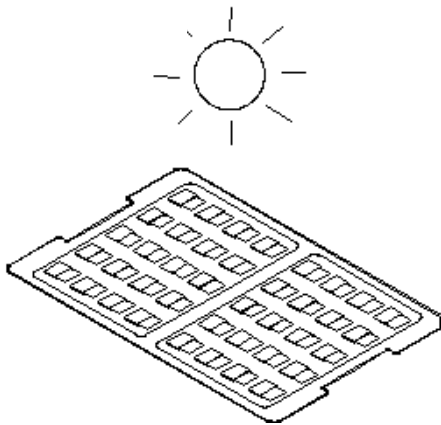
### [For operating LCD module]

- (1) Do not operate or store the LCD module under outside of specified environmental conditions.
- (2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
- (3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

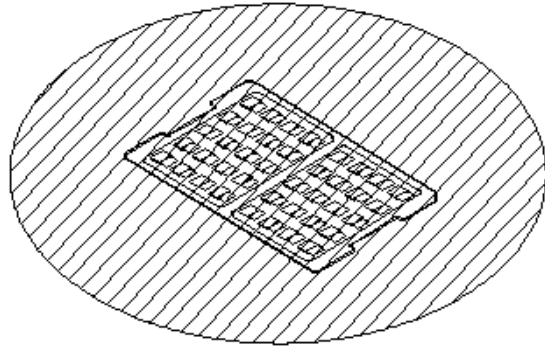
### [Precautions for Storage]

- (1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
- (2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
- (3) Keeping Method
  - a. Don't keeping under the direct sunlight.
  - b. Keeping in the tray under the dark place.

## DON'T



## DO



- (4) Do not operate or store the LCD module under outside of specified environmental conditions.
- (5) Be sure to prevent light striking the chip surface.

### [Other Notice]

- (1) Do not operate or store the LCD module under outside of specified environmental conditions.
- (2) As electrical impedance of power supply lines (VDDI-GND) are low when LCD module is working, place the de-coupling capacitor nearby LCD module as close as possible.
- (3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.
- (4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.
- (5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.
- (6) No bromide specific fire-retardant material is used in this module.
- (7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.
- (8) U/V glue (Liquid OCA) should not be attached on upper polarizer edge, when customer laminate cover glass and touch panel on LCD.

### [Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

## 1. Application

This data sheet is to introduce the specification of active matrix 16,777,216 color LCD module.

Main color LCD module is controlled by Driver IC (R63423).

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

As to basic specification of driver IC refer to the IC specification and handbook.

## 2. Construction and Outline

This module is a color transmissive, high contrast, wide viewing angle and active matrix LCD module incorporating CG-Silicon TFT (Continuous Grain-Silicon Thin Film Transistor).

Construction: LCD panel, Driver (COG), FPC with electric components, LEDs, prism sheet, diffuser, light guide, reflector and plastic frame to fix them mechanically.

Outline: See page 30 (Fig.18 Outline dimensions)

Connection: Board-to-Board Plug Connector (JAE WP7B-P040VA1)

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

Rejection criteria shall be noted in Inspection Standard.

## 3. Mechanical Specification

Table 1

Item	Specifications	Unit	Remarks
Screen size	73.406 (2.89" type) Diagonal	mm	
Active area	51.84(H)X51.84(V)	mm	
Pixel format	1440(H)X1440(V)	Pixel	
	1 Pixel =R+G+B dots	-	
Pixel pitch	0.012 (H) x 0.036(V)	mm	
Pixel configuration	R,G,B vertical stripes	-	
Display mode	Normally Black	-	
LDC Driving method	DC Driving / Column	-	
Liquid Crystal Mode	New Mode2	-	
Number of colors	16,777,216	Colors	24 bits
Outline dimensions	54.24 X 59.02 X 1.365	mm	Note 3-1
Mass	7	g	

Note 3-1) The above-mentioned table indicates module sizes without some projections and FPC.

## 4. Pixel Configuration

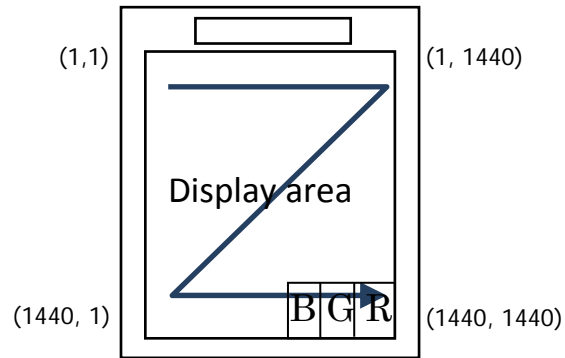


Fig. 1



## 5. Input Terminal Names and Functions

Table 2

Pin No	Symbol	I/O	Description	Remarks
1	DSIA_D3_N	I	MIPI data3 negative signal of MIPI Port A	
2	DSIA_D3_P	I	MIPI data3 positive signal of MIPI Port A	
3	DSIA_D0_N	I/O	MIPI data0 negative signal of MIPI Port A	
4	DSIA_D0_P	I/O	MIPI data0 positive signal of MIPI Port A	
5	DSIA_CLK_N	I	MIPI clock negative signal of MIPI Port A	
6	DSIA_CLK_P	I	MIPI clock positive signal of MIPI Port A	
7	DSIA_D1_N	I	MIPI data1 negative signal of MIPI Port A	
8	DSIA_D1_P	I	MIPI data1 positive signal of MIPI Port A	
9	DSIA_D2_N	I	MIPI data2 negative signal of MIPI Port A	
10	DSIA_D2_P	I	MIPI data2 positive signal of MIPI Port A	
11	DSIB_D2_P	I	MIPI data2 positive signal of MIPI Port B	
12	DSIB_D2_N	I	MIPI data2 negative signal of MIPI Port B	
13	DSIB_D1_P	I	MIPI data1 positive signal of MIPI Port B	
14	DSIB_D1_N	I	MIPI data1 negative signal of MIPI Port B	
15	DSIB_CLK_P	I	MIPI clock positive signal of MIPI Port B	
16	DSIB_CLK_N	I	MIPI clock negative signal of MIPI Port B	
17	DSIB_D0_P	I/O	MIPI data0 positive signal of MIPI Port B	
18	DSIB_D0_N	I/O	MIPI data0 negative signal of MIPI Port B	
19	DSIB_D3_P	I	MIPI data3 positive signal of MIPI Port B	
20	DSIB_D3_N	I	MIPI data3 negative signal of MIPI Port B	
21	EN1PORT	I	EN1PORT is used for enable or disable MIPI dual port	"H" single port
22	AVDD	-	Power supply for analog	
23	VDDI	-	Power supply for I/O	
24	VDDI	-	Power supply for I/O	
25	EXCK	I	External Clock (not used)	GND
26	GND	-	Ground	
27	GND	-	Ground	
28	GND	-	Ground	
29	RESX	I	Device reset signal	"L" Active
30	FTE	O	Frame head pulse signal (not used)	Open
31	Sync	O	Synchronizing signal (not used)	Open
32	LEDPWM	O	Backlight LED driver PWM (if not used, "floating")	
33	AGND	-	Ground	
34	AGND	-	Ground	-
35	AGND	-	Ground	I
36	AVEE	-	Power supply for analog	I
37	LED_CA1		LED back light power negative1	I
38	LED_CA2		LED back light power negative2	I
39	LED_AN1		LED back light power positive1	-
40	LED_AN2		LED back light power positive2	-

Fitting connector: JAE WP7B-S040VA1 (Board-to-Board Receptacle)

Pin layout: See Outline dimensions. (P.30)

Recommended outside circuit:

<MIPI DSI (Single Port)>

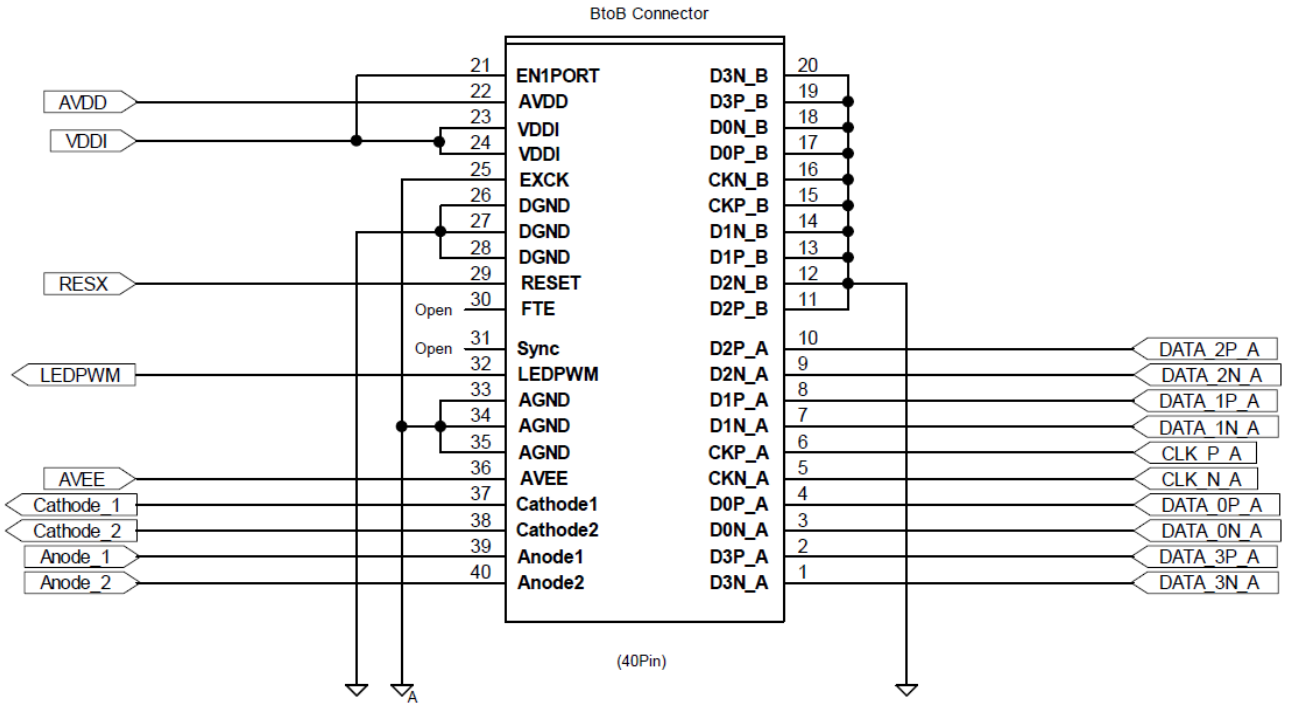


Fig. 2

## 6. Absolute Maximum Ratings

Table3

GND=0V

Parameter	Symbol	Conditions	Rated value	Unit	Remarks
Driver IC (Positive Analog) Power Supply Voltage	AVDD	Ta=+25°C	-0.3 to +6.5	V	Note6-1
Driver IC (Negative Analog) Power Supply Voltage	AVEE	Ta=+25°C	+0.3 to -6.5	V	Note6-1
Driver IC (Digital) Power Supply Voltage	VDDI	Ta=+25°C	-0.3 to +5.5	V	Note6-1
Temperature for storage	Tstg	-	-30 to +70	°C	Note6-2
Temperature for operation	Topr	-	-20 to +60	°C	Note6-2
LED Input electric current	ILED	Ta=+25°C	25	mA	Note6-3

Note6-1) Voltage applied to GND pins. GND pin conditions are based on all the same voltage (0V).

Always connect all GND externally and use at the same voltage.

Note6-2) Humidity: 95%RHMax.(at Ta≤40°C). Maximum wet-bulb temperature is less than 39°C (at Ta>40°C).

Condensation of dew must be avoided.

Note6-3) Ambient temperature and the maximum input are fulfilling the following operating conditions.

Ambient Temperature vs  
Allowable Forward Current

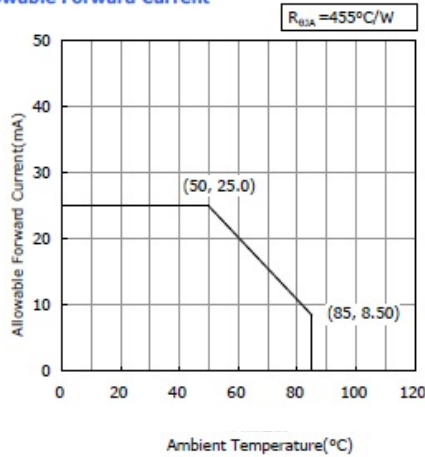


Fig. 3

## 7. Electrical Specifications

### 7-1. TFT-LCD Panel Driving Section

Table4

Ta=+25°C, GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Driver IC(Digital) Power Supply Voltage	VDDI	1.70	1.80	1.9	V	Note7-1
Driver IC(Positive Analog) Power Supply Voltage	AVDD	5.3	5.5	6.0	V	Note7-1
Driver IC(Negative Analog) Power Supply Voltage	AVEE	-6.0	-5.5	-5.3	V	Note7-1
Input voltage (Low)	V <sub>IL</sub>	0	-	0.3 VDDI	V	Note7-2
Input voltage (High)	V <sub>IH</sub>	0.7 VDDI	-	VDDI	V	Note7-2
Input current (Low)	I <sub>IL</sub>	-10	-	-	μA	
Input current (High)	I <sub>IH</sub>	-	-	10	μA	
Output voltage (Low)	V <sub>OL</sub>	0	-	0.2 VDDI	V	I <sub>OL</sub> =+0.1mA
Output voltage (High)	V <sub>OH</sub>	0.8 VDDI	-	VDDI	V	I <sub>OH</sub> =-0.1mA
Current consumption Video mode without RAM 2port(SDC)	I <sub>VDDIO</sub>	-	33(*1)	65(*3)	mA	Note7-3
	I <sub>VSP</sub>	-	20(*1)	40(*2)	mA	
	I <sub>VSN</sub>	-30(*3)	-12(*1)	-	mA	

Note7-1) Include Ripple Noise

Note7-2) Applied overshoot

Note7-3) 120Hz / (\*1) Gradation shift pattern, (\*2) 1dot checker pattern, (\*3) Random dot pattern

### 7-2. Back Light Driving Section

Table5

Ta=+25°C, GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
LED Voltage	V <sub>LED</sub>	-	2.9	3.2	V	per unit
LED Current	I <sub>LED</sub>	-	11	20	mA	
Power Consumption	W <sub>LED</sub>	-	255.2	-	mW	
LED Quantity			8		pcs	

## 8. Timing characteristics of input signals

### 8-1. MIPI DC/AC Characteristics

<DC characteristics>

Table6

	Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	70	
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-70	-	-	
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 1.95V	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC=1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	450	-	-	

- Notes: 1.  $V_{CMRX}(DC) = (V_P + V_{DN})/2$   
 2. Excluding COG resistance (contact resistance and ITO wiring resistance).

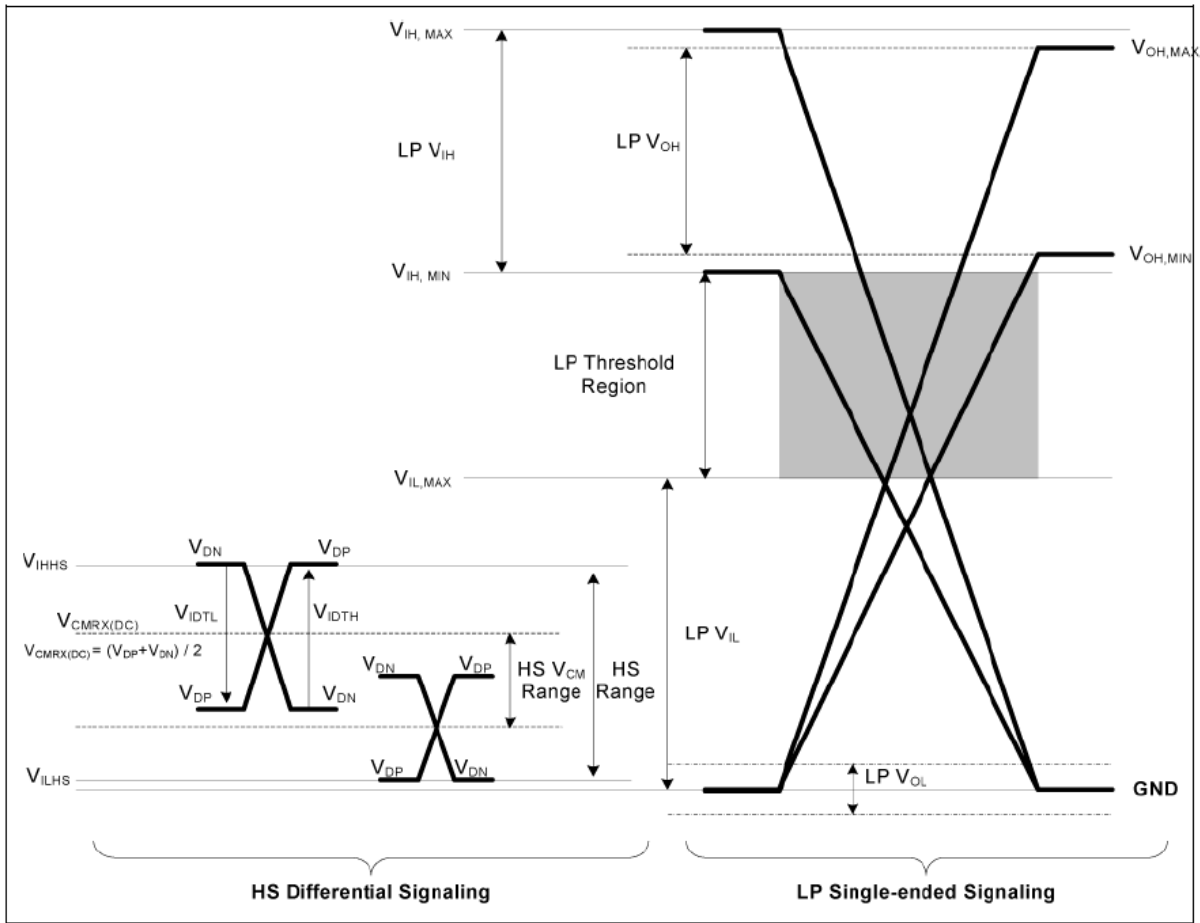


Fig. 4

<AC Characteristics>

MIPI DSI HS-RX Clock and Data-Clock Specifications

Table7

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	2	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6

- Notes:
- When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
  - Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
  - tSETUP/tHOLD Time is measured without HS-TX Jitter.

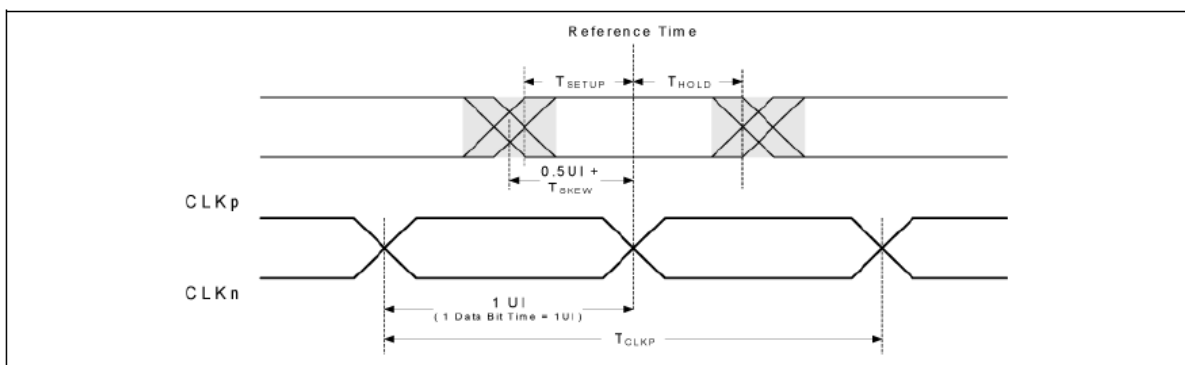


Fig. 5

## MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Table8

Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE} + T_{HS-ZERO}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	max ( $n*8*UI$ , 60 ns + $n*4*UI$ )	-	-	1,2
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	100	-	-	
Time to drive LP-00 after Turnaround Request	$T_{TA-GO}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	4* $T_{LPTX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	1* $T_{LPTX}$	-	2* $T_{LPTX}$	
Time to drive LP-00 by new TX	$T_{TA-GET}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	5* $T_{LPTX}$			
Length of any Low-Power state period	$T_{LPX}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	50	-	-	
Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	Ratio $T_{LPX}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	$T_{EOT}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	-	-	105 ns + $n*12*UI$	2
Length of Low-Power TX period in case of using DSI clock	$T_{LPTX1}$	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	$T_{LPTX2}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	1/(fosc/4)	-	

- Notes:
- If  $a > b$  then  $\max(a, b) = a$ , otherwise  $\max(a, b) = b$
  - Where  $n = 1$  for Forward-direction HS mode.
  - The R63423 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63423 can work without the remained process if  $t_{CLK-POST}$  is more than 512 UI.
  - The R63423 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled.



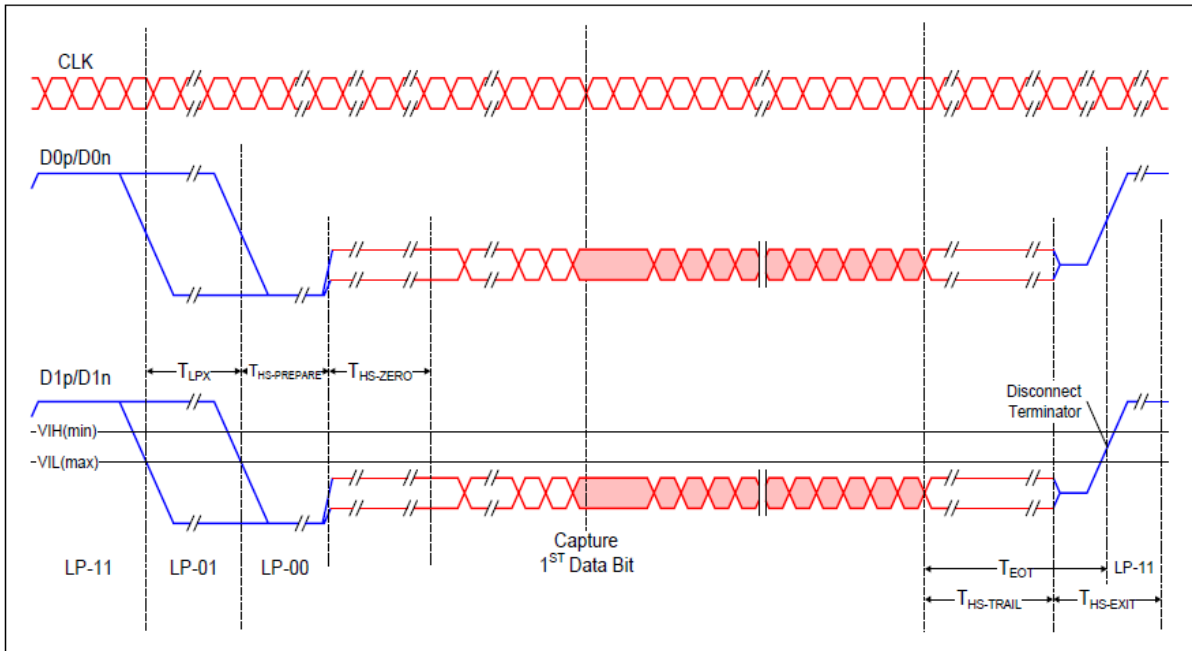


Fig. 6

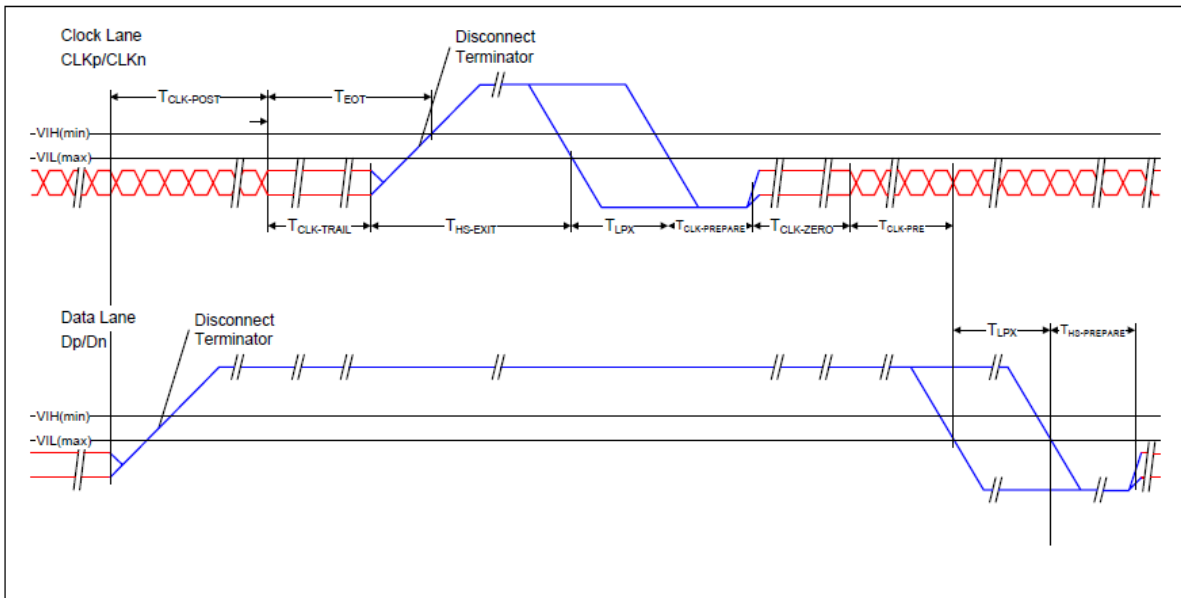


Fig. 7

## 8-2 Reset Timing Characteristics

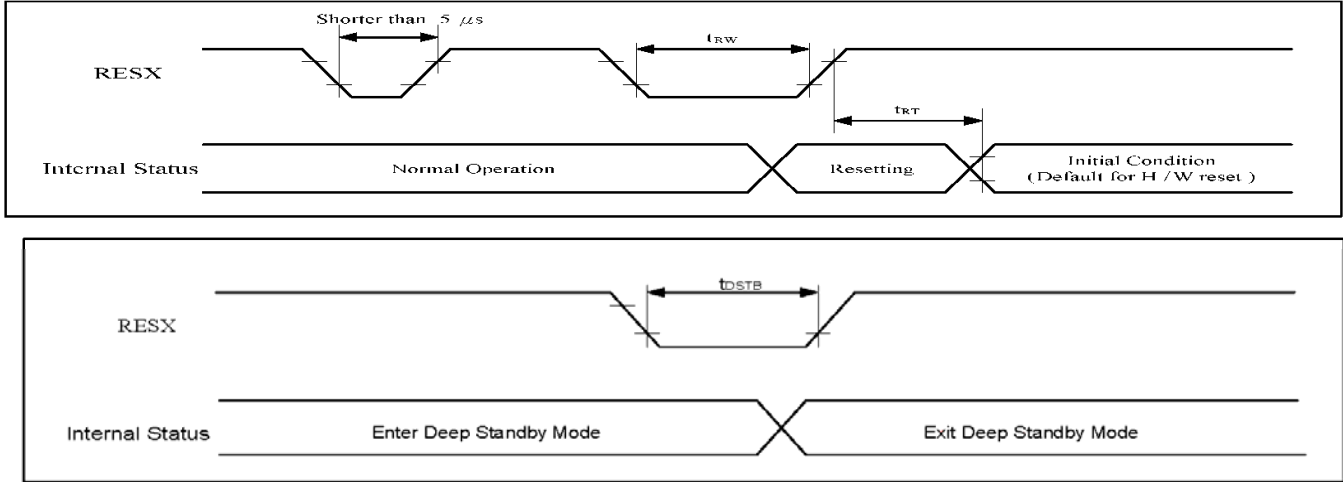


Figure 8

Table 9

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	$t_{RW}$	Reset pulse duration	10(Note)	-	us
	$t_{RT}$	Reset cancel	-	10(Note)	ms
			-	120(Note)	ms
$t_{DSTB}$	Reset pulse duration	3	-	ms	

Note :

-The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers.

This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 10 ms after a rising edge of RESX.

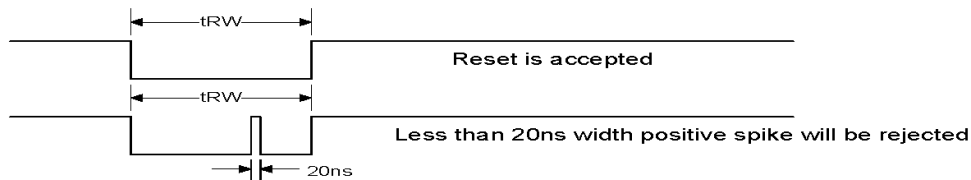
-Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :

Table10

RESX	Pulse Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

-During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-Spike Rejection also applies during a valid reset pulse as shown below :



-When Reset applied during Sleep-In Mode.

-When Reset applied during Sleep-Out Mode.

-It is necessary to wait 10ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

### 8-3 Display timing

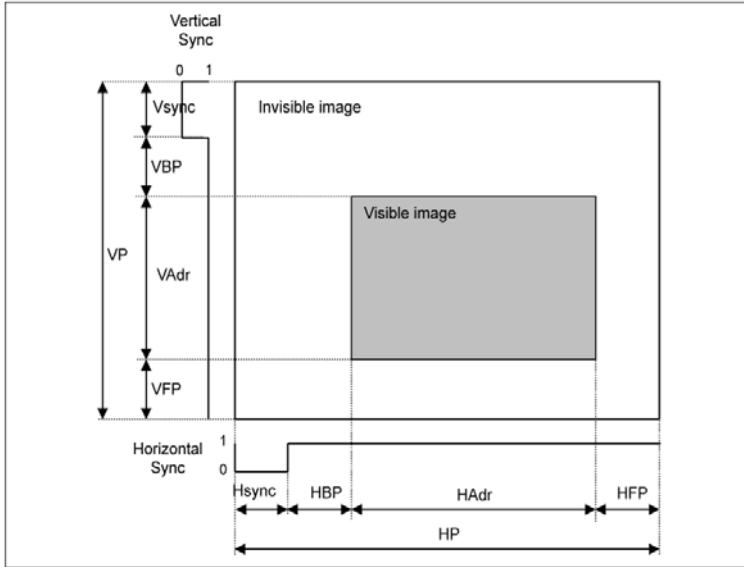


Figure 9

< Interface Display timing (60Hz, no compression) >

Table11

I/F:MIPI DSI 4lane, Dots Size:1440xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		24		Pixel
Horizontal active area (HAdr)		1440		Pixel
Horizontal front porch(HFP)		24		Pixel
Vertical low pulse width(VS)		1		H
Vertical front porch(VFP)		8		H
Vertical back porch(VBP)		7		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(58.2)	60	(61.8)	Hz
1H Time	(11.103)	11.446	(11.790)	us
DSI DATA rate	(756.6)	(780.0)	(803.4)	Mbps/Lane

<Interface Display timing (90Hz, with 1/2 compression) \*>

Table12

I/F:MIPI DSI 4lane, Dots Size:1440xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		20		Pixel
Horizontal active area (HAdr)		720		Pixel
Horizontal front porch(HFP)		38		Pixel
Vertical low pulse width(VS)		2		H
Vertical front porch(VFP)		8		H
Vertical back porch(VBP)		6		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(87.3)	90	(92.7)	Hz
1H Time	(7.092)	7.31	(7.552)	us
DSI DATA rate	(593.6)	(612.0)	(630.4)	Mbps/Lane

\*For TC358860XBG (Toshiba)

<Interface Display timing (120Hz, with 1/2 compression) \*>

Table13

I/F:MIPI DSI 4lane, Dots Size:1440xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		20		Pixel
Horizontal active area (HAdr)		720		Pixel
Horizontal front porch(HFP)		38		Pixel
Vertical low pulse width(VS)		2		H
Vertical front porch(VFP)		8		H
Vertical back porch(VBP)		6		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(118.8)	120	(121.2)	Hz
1H Time	(5.663)	5.721	(5.778)	us
DSI DATA rate	(807.8)	(816.0)	(824.1)	Mbps/Lane

\*For TC358860XBG (Toshiba)

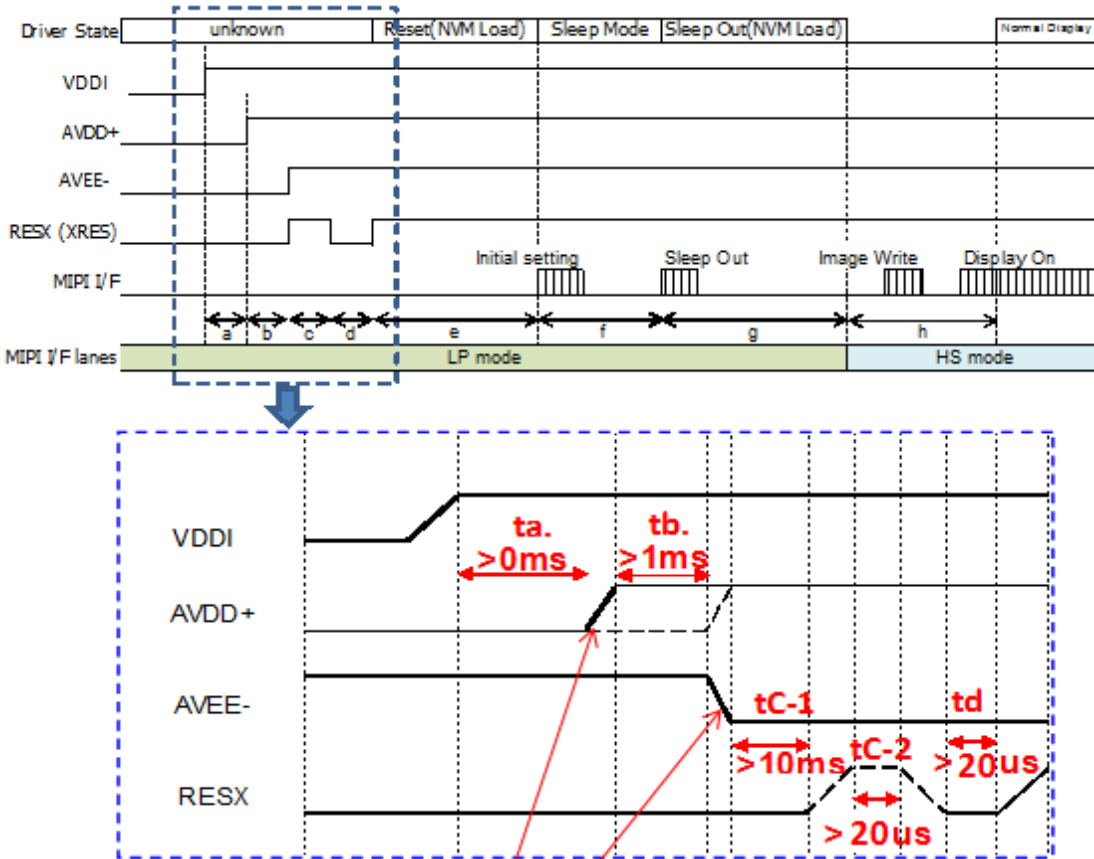
Table14

Additional Command for 90Hz and 120Hz (Please insert below into Power On Sequence "step.15")

Address	Value	Data Type	Comment
EB	82	Genelic long WRITE , 2parameter	1/2 Compression Support
	00		

## 9. Power Sequence

### 9-1 Power on sequence



Note:With the destination of avoiding latch-up issue,  
the AVDD/AVEE slope time should set  $>0.2ms$

Figure 10

Table 15: Recommended Power On Sequence

Step	Address	Parameter	Data	DSI data type	Delay	Command	
1	Initial condition					XRES = L	
2	Power Supply VDDI (Typ. 1.8V)					VDDI ON	
3	Wait				Min.>0ms	(a.) Wait until VDDI power stable	a.
4	Power Supply AVDD+ (Typ. +5.5V)					AVDD+ ON	
5	Wait				Min.>1ms	(b.) After wait until AVDD+ power stable (rising slope > 0.2ms)	b.
6	Power Supply AVDD- (Typ. -5.5V)					AVDD- ON	
7	Wait				Min. 10ms	(c.) After Wait until AVDD- power stable (rising slope > 0.2ms)	c-1.
8	RESX High					XRES = H	
9	Wait				Min. 20us		c-2.
10	RESX go Low					XRES = L	
11	Wait				Min. 20us		d.
12	RESX go High					XRES = H	
13	Wait				Min. 10ms	[Automatic] NVM Auto load	e.
14						[Automatic] Sleep Mode On	
15	11h	-	-	DCS 05h		Sleep Out	
16	Wait				Min. 100ms		
17						[Automatic] Sleep Mode Off	
18	Display data transfer					Image Write	g.
19	29h	-	-	DCS 05h		Display On	
20	Wait				Min. 40ms		
21						[Automatic] Display On	
22	Backlight on						

## 9-2 Power off sequence

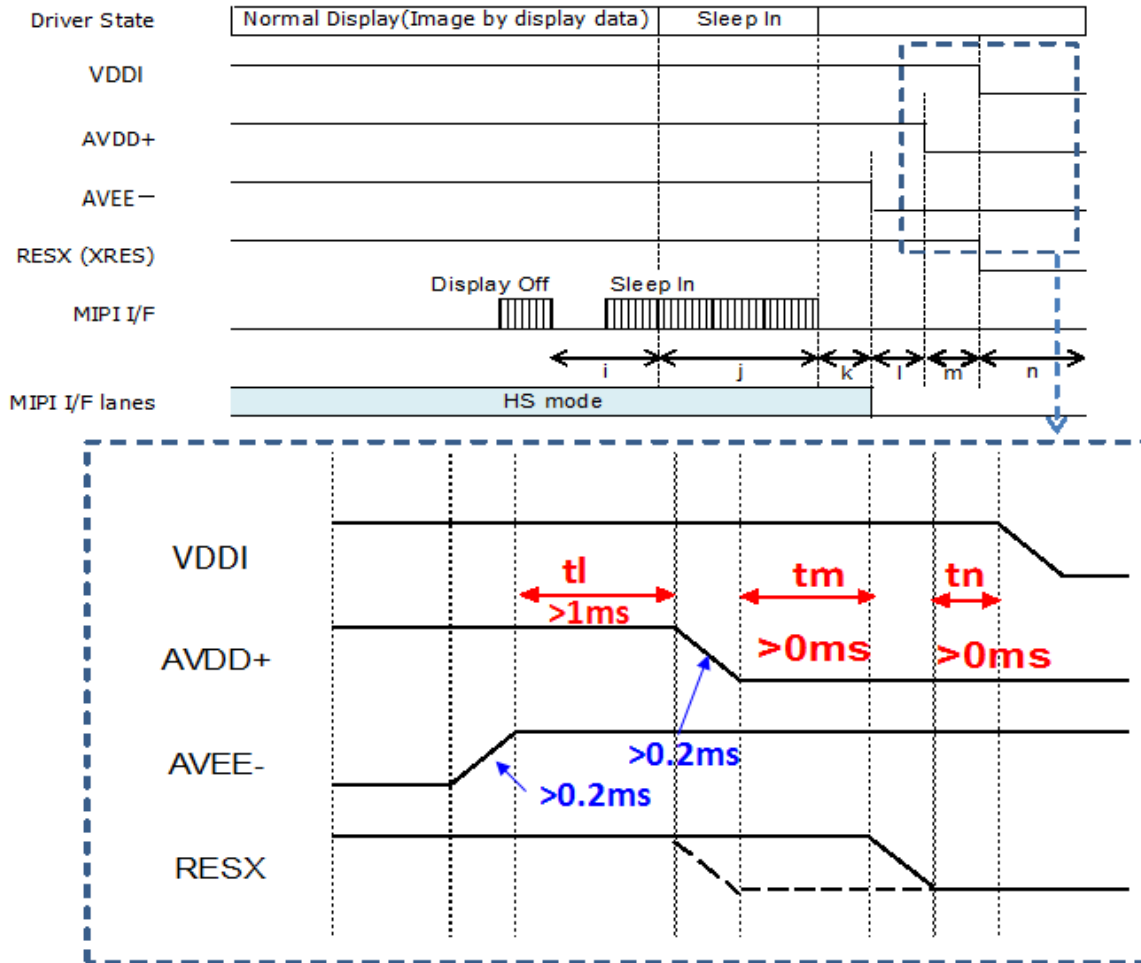


Figure 11

Table16: Recommended Power Off Sequence

Step	Address	Parameter	Data	DSI data type	Delay	Command	
1	28h	-	-	DCS 39h		Display Off	g
2	Wait				Min.1 frame		
3	10h	-	-	DCS 39h		Sleep In	h
4	Wait				Min.4 frame	Hsync/Vsync signals should be send after Sleep In command	
5						Mipi data transfer Stop	
6		AVEE-(Typ -5.5V) OFF					k
7					tPOFF1/tPOFF2	Wait	
8		AVDD+(Typ +5.5V) OFF					m
9					thAVP	Wait	
10		RESX Low				XRES = L	j
11	Wait				Min.0ms		
12		VDDI OFF (Typ.1.8V) OFF					

## 10. Input Signals, Basic Display Colors and Gray Scale of Each Color

Table 17

0: Low level voltage, 1: High level voltage

Colors & Gray Scale	Gray Scale	Data signals																																				
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7													
		LSB							MSB							LSB							MSB															
Basic Color	Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Blue	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Green	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Cyan	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Red	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
	Magenta	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
	Yellow	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	↑	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	↓																																				
	↓	↓																																				
	Brighter	GS253	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	↓	GS254	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Red	GS255	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	↑	↓																																				
	↓	↓																																				
	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	↓	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	↓																																				
	↓	↓																																				
	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↓	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Each basic color can be displayed in 256 gray scales from 8 bit data signals. According to the combination of total 24 bit data signals, the 16,777,216-color display can be achieved on the screen.



## 11. Optical Characteristic

Table18

VDDI=1.8V, AVDD=5.5V, AVEE=-5.5V, ILED=11mA/pcs, Ta = 25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	$\theta=0^\circ$	770	1100	-	-	Note11-1,2
Response Time	$\tau_r + \tau_d$	$\theta=0^\circ$	-	10	-	ms	Note11-3
White Chromaticity	x	$\theta=0^\circ$	0.240	0.290	0.340	-	
	y		0.265	0.315	0.365	-	
Red Chromaticity	x		0.615	0.665	0.715	-	
	y		0.260	0.310	0.360	-	
Green Chromaticity	x		0.210	0.260	0.310	-	
	y		0.545	0.595	0.645	-	
Blue Chromaticity	x		0.095	0.145	0.195	-	
	y		0.045	0.095	0.145	-	
Viewing Angle	$\theta_{11}, \theta_{12}, \theta_{21}, \theta_{22}$	CR>10	80	-	-	degree	Note11-1,2
Brightness	L	$\theta=0^\circ$	210	300	-	cd/m <sup>2</sup>	I <sub>LED</sub> =11mA
Uniformity	U	$\theta=0^\circ$	70		-	%	Note11-4
NTSC Ratio	S	$\theta=0^\circ$	-	75	-	%	
Gamma	$\gamma$	$\theta=0^\circ$	1.8	2.2	2.6	-	
Flicker	F	$\theta=0^\circ$	-	-	30	%	Note11-5
Crosstalk	CT	$\theta=0^\circ$	-	-	5	%	Note11-6

\*The measuring method of the optical characteristics is shown by the following figure.

\*A measurement device is TOPCON luminance meter SR-3. (Measurement angle 1°)

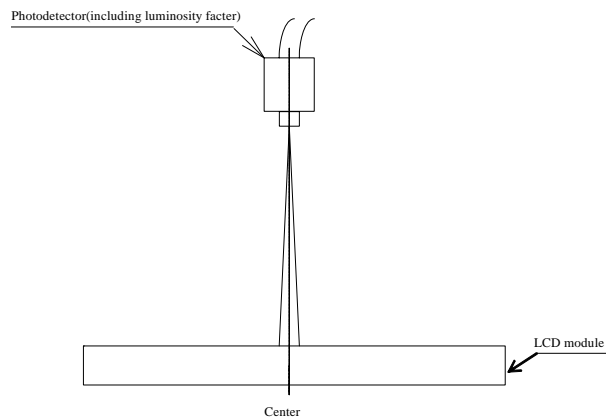


Fig.12

Note 11-1) Contrast / NTSC / GAMMA viewing angle is defined as follows.

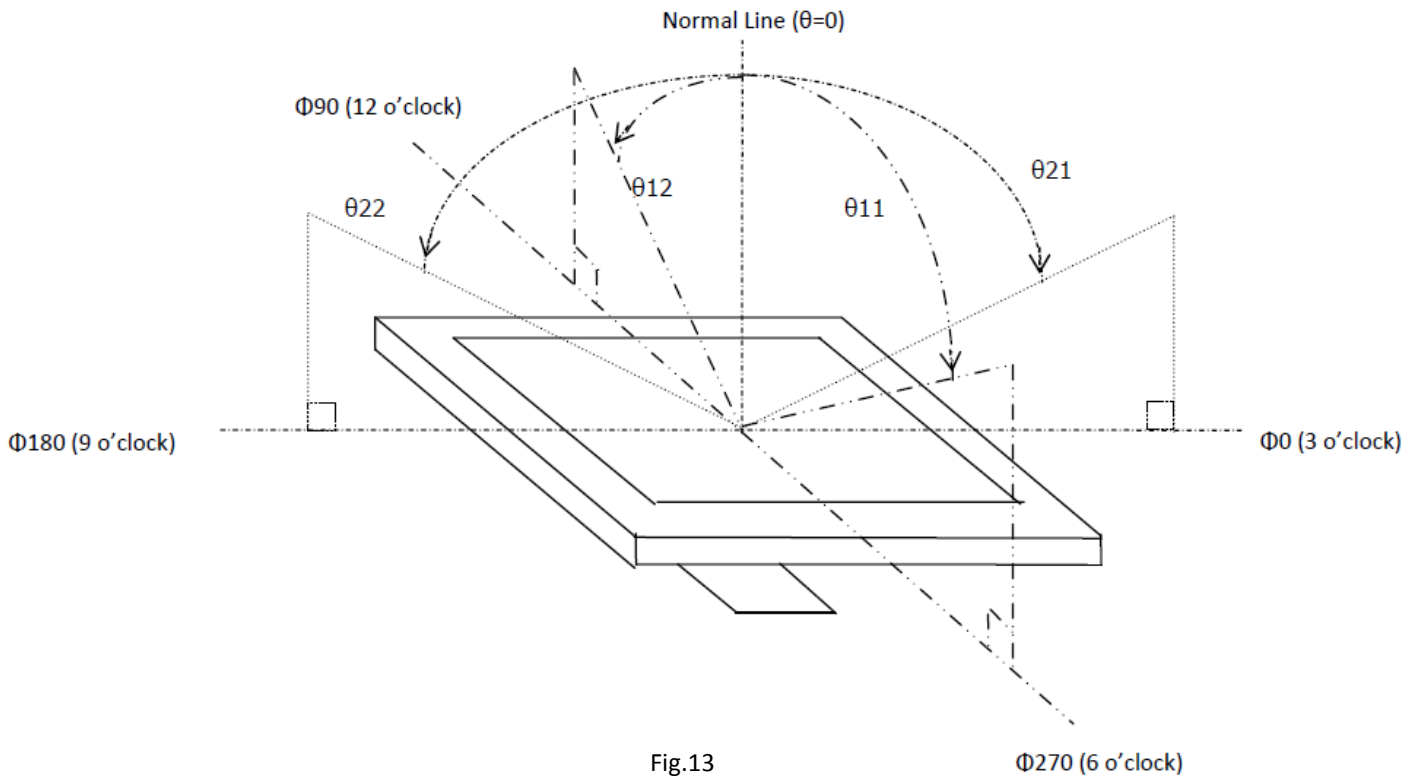


Fig.13

Note 11-2) Definition of contrast ratio:

The contrast ratio is defined as the follows:

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance(brightness) with all pixels white}}{\text{Luminance(brightness) with all pixels black}}$$

Note 11-3) Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”

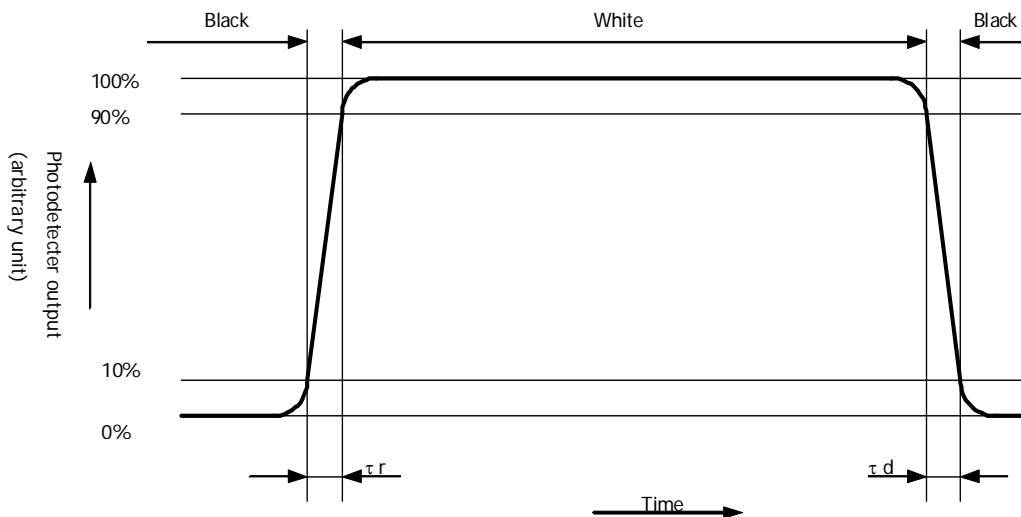


Fig.14

Note 11-4) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

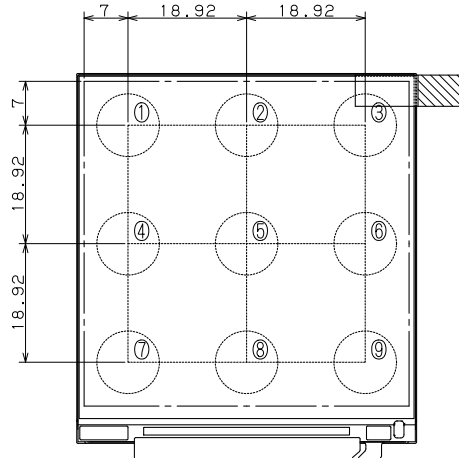


Fig.15

Note 11-5) Measuring systems: Konica-Minolta CA-310

- Temperature = 25°C (±3°C), Frame Frequency = 57Hz~63Hz, LED back-light: ON, Environment brightness < 150 lx
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.
- Measuring pattern Please refer to figure below.

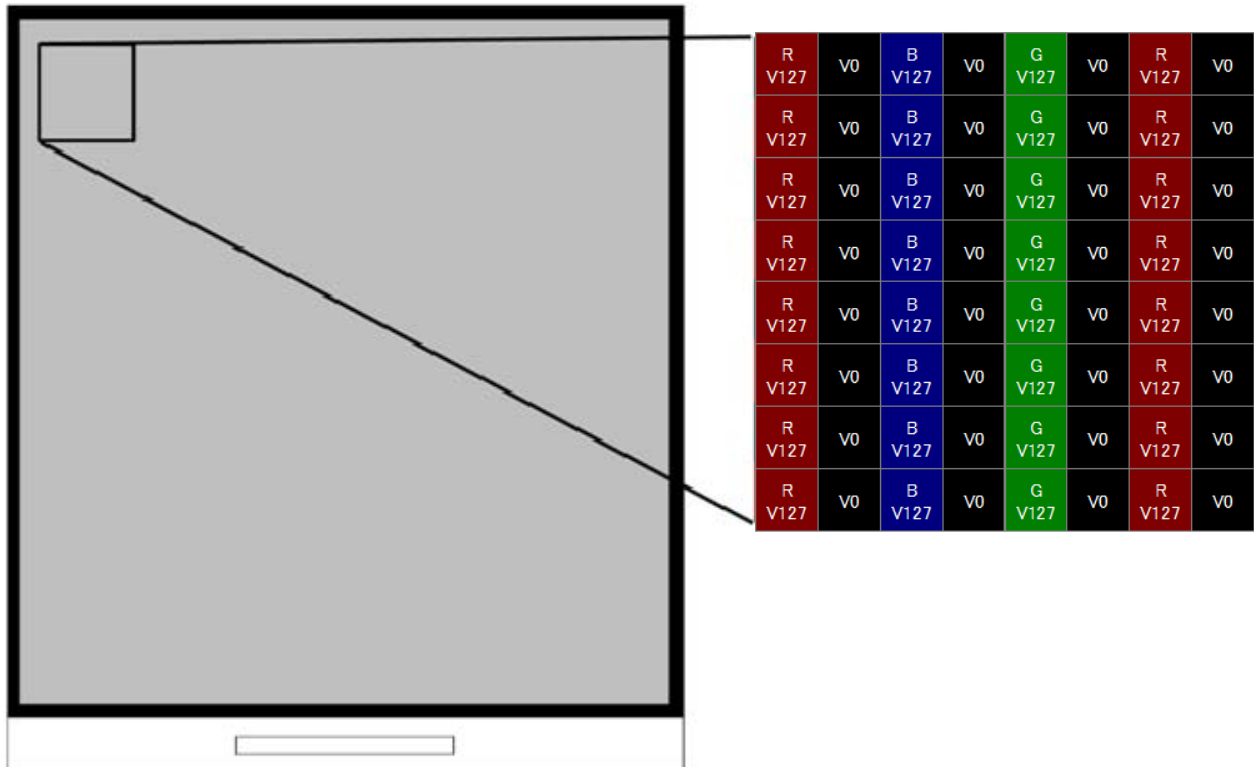


Fig.16

Note 11-6) Definition of Crosstalk

$$CT_B = \frac{|Y_B(x) - Y_G(x)|}{Y_G(x)} \times 100 (\%)$$

$$CT_W = \frac{|Y_W(x) - Y_G(x)|}{Y_G(x)} \times 100 (\%)$$

x=U, D, L or R

Gray level=V128

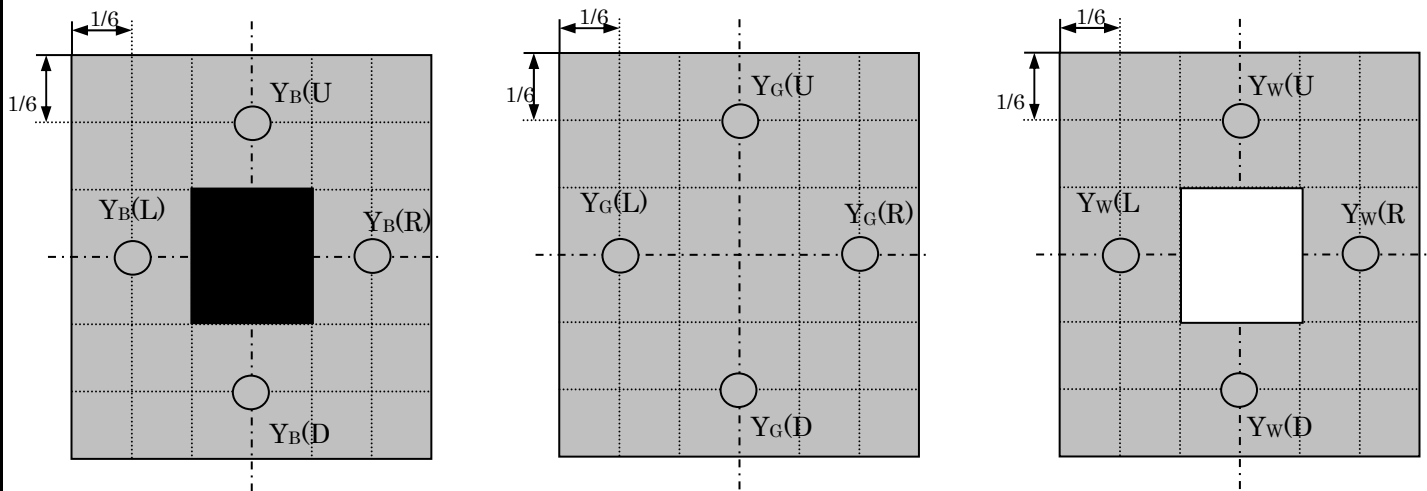


Fig.17

## 12. Reliability

Table 19

No.	Test item	Conditions
1	High temperature storage test	Ta = +80°C, 200h
2	Low temperature storage test	Ta = -30°C, 200h
3	High temperature operation test	Ta = +70°C, 120h
4	Low temperature operation test	Ta = -20°C, 120h
5	High temperature and high humidity operation test	Ta = +50°C90%RH, 120h (No condensation)
6	Heat shock test	Ta = -20°C(30min) ~ 70°C(30min), 10 cycle
7	Electro static discharge test	±200V, 200pF(0Ω) to Terminals(Contact) (1 time for each terminals) None Operation
8	Packing Vibration test	Frequency: 5 to 50Hz (Round trip 3 minutes) Acceleration: 1G All Amplitude: 20 to 0.2mm Direction: Up/Down(60min), Left/Right(15min), Front/Back(15min) (3 Direction)  Amplitude 20mm 0.2mm 20mm 0.2mm Frequency 5Hz 50Hz 5Hz 50Hz ○———○———○———○  ← 3 minutes →
	Packing Drop test	Height: 75cm, Drop times: 10 Drop (1 Conner,3 Edges and 6 Faces)

Note 12-1) Ta = Ambient temperature

Note 12-2) Check items for other Test

In the standard condition, there shall be no practical problems that may affect the display function.

### 13. Indication of lot number

Attached location is shown in Fig. 30 Outline dimensions.

The lot number is shown on a label.

**LS029B3SX02**  
**F Y M D P XXXXX R**

#### \*Detail of S/N

LS029B3SX02 : Sharp model number

F : Factory code / STECH=E, Other=J

Y : Manufacture year / 2015 = 5, 2016 = 6

M : Manufacture month / January= 1, --- September= 9, October= A --- December=C

D : Manufacture month / 1st= 1, --- 9th= 9, 10th= A --- 31th=X

P : ID number of Printer

XXXXX : Serial number (5 digits) / 00001~99999

R : Revision code / A, B, -----

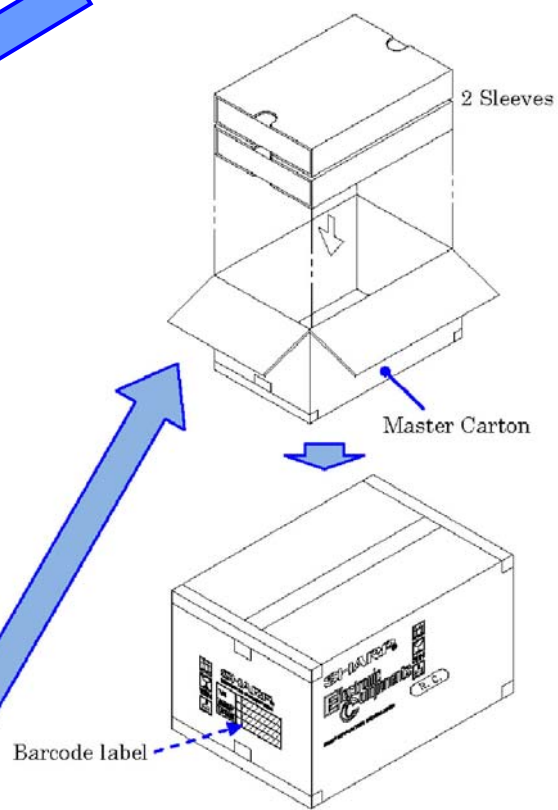
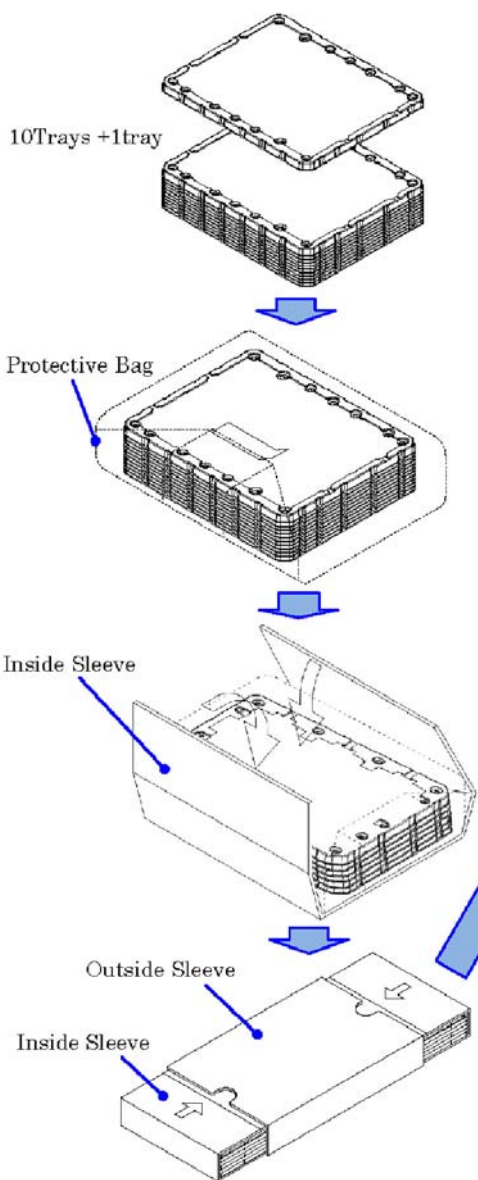
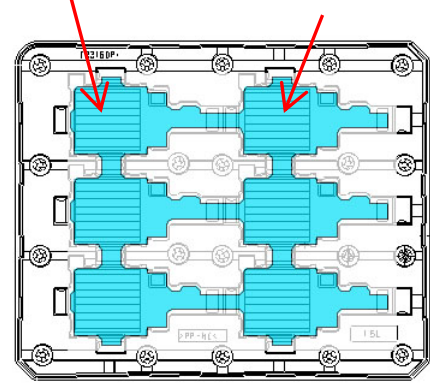
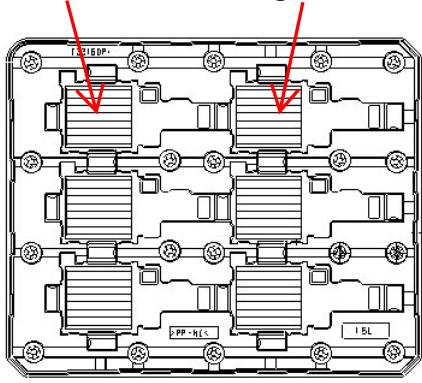
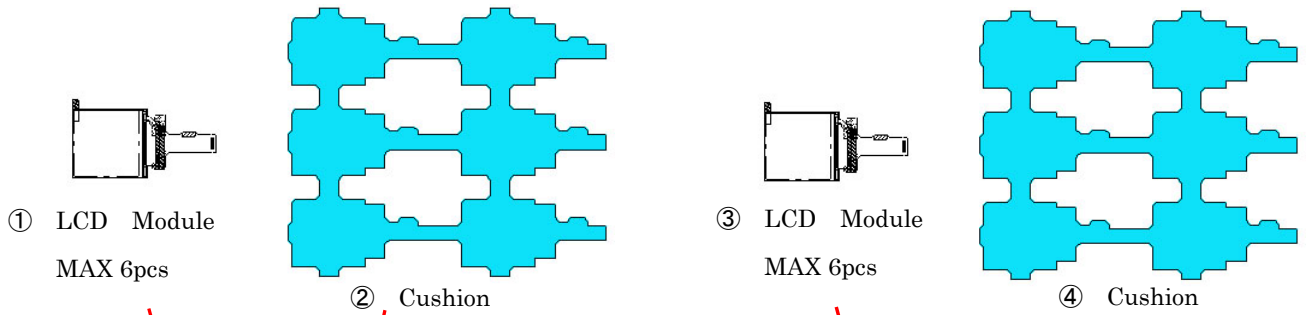
### 14. Forwarding form

- (a) Piling number of cartons: 8 deep
- (b) Package quality in one cartons: 480 pcs
- (c) Carton size: 580mm × 365mm × 279mm
- (d) Total mass of 1 carton filled with full modules: approximately 9.3 kg

#### Condition for storage

##### Environment

- (1) Temperature: 0 to 40°C
- (2) Humidity: 60%RH or less (at 40°C)
- (3) Atmosphere: Harmful gas, such as acid or alkali which erodes electronic components and/or wires, must not be detected.
- (4) Period: about 3 months
- (5) Opening of the package: In order to prevent the LCD module from breakdown by electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as earth, etc.



## Outline dimensions

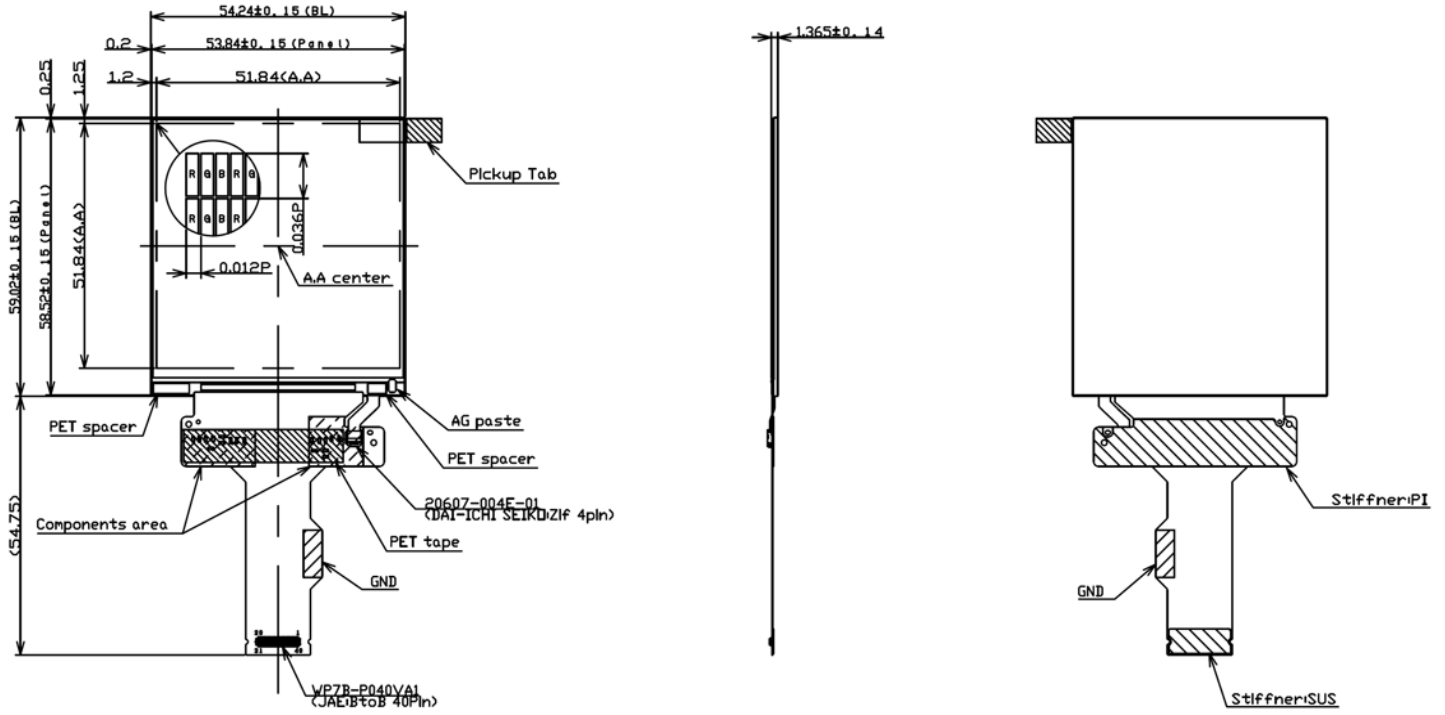


Figure 18



## FPC Schematic

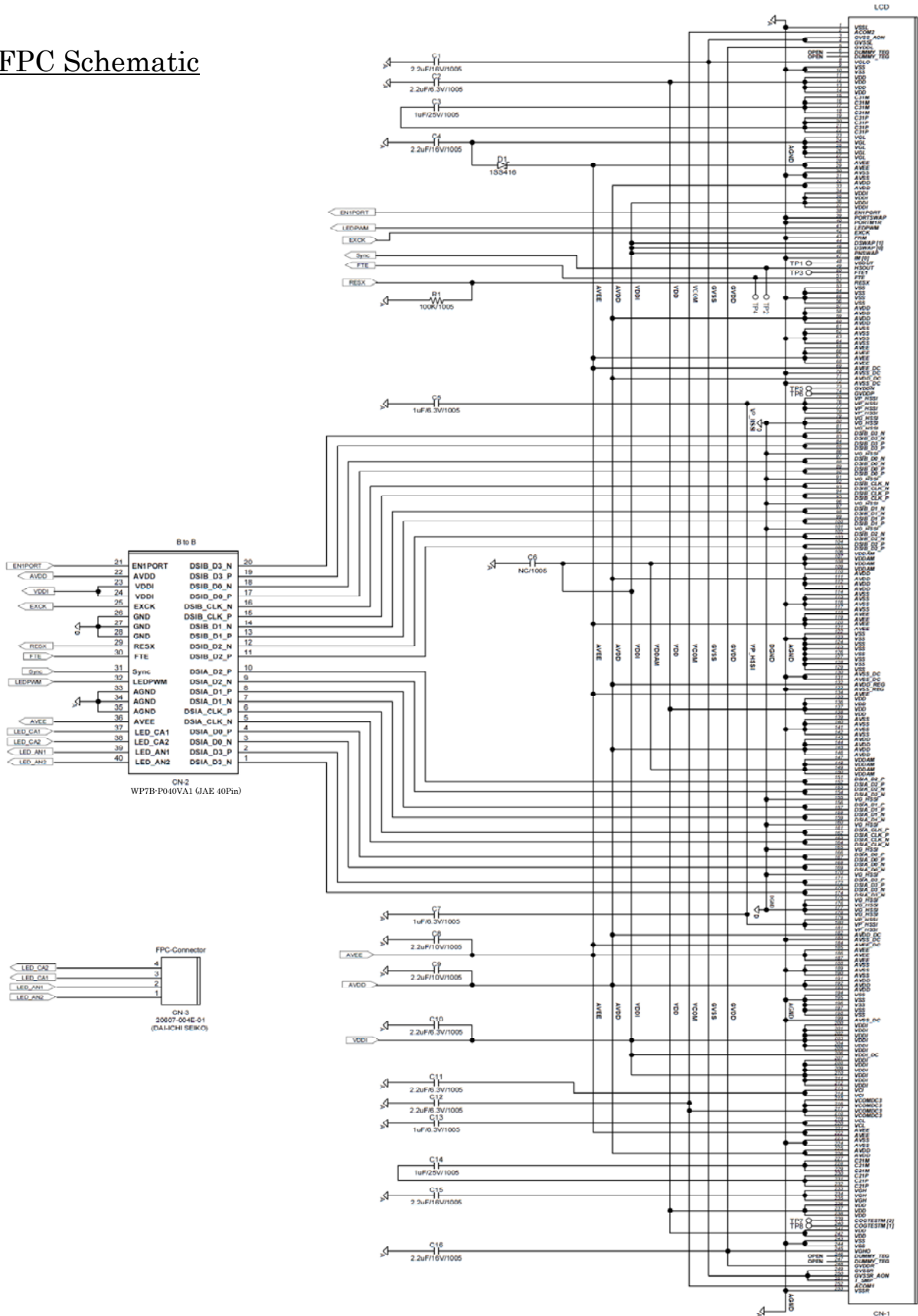


Figure 19